

035217-10000000

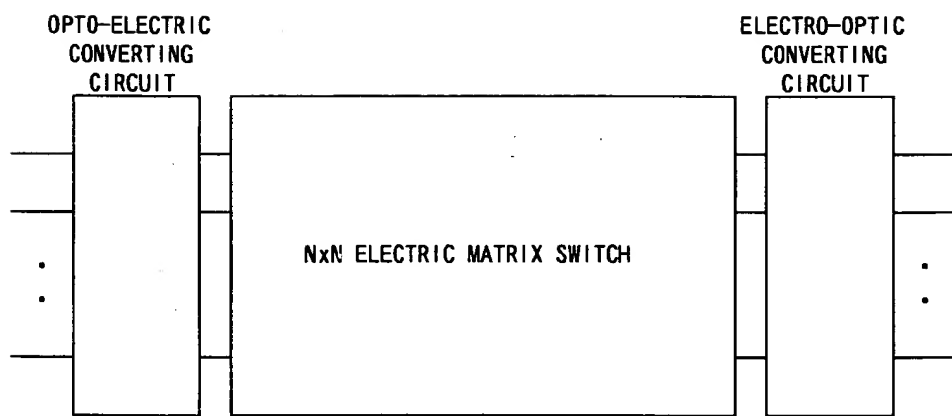


FIG. 2 PRIOR ART

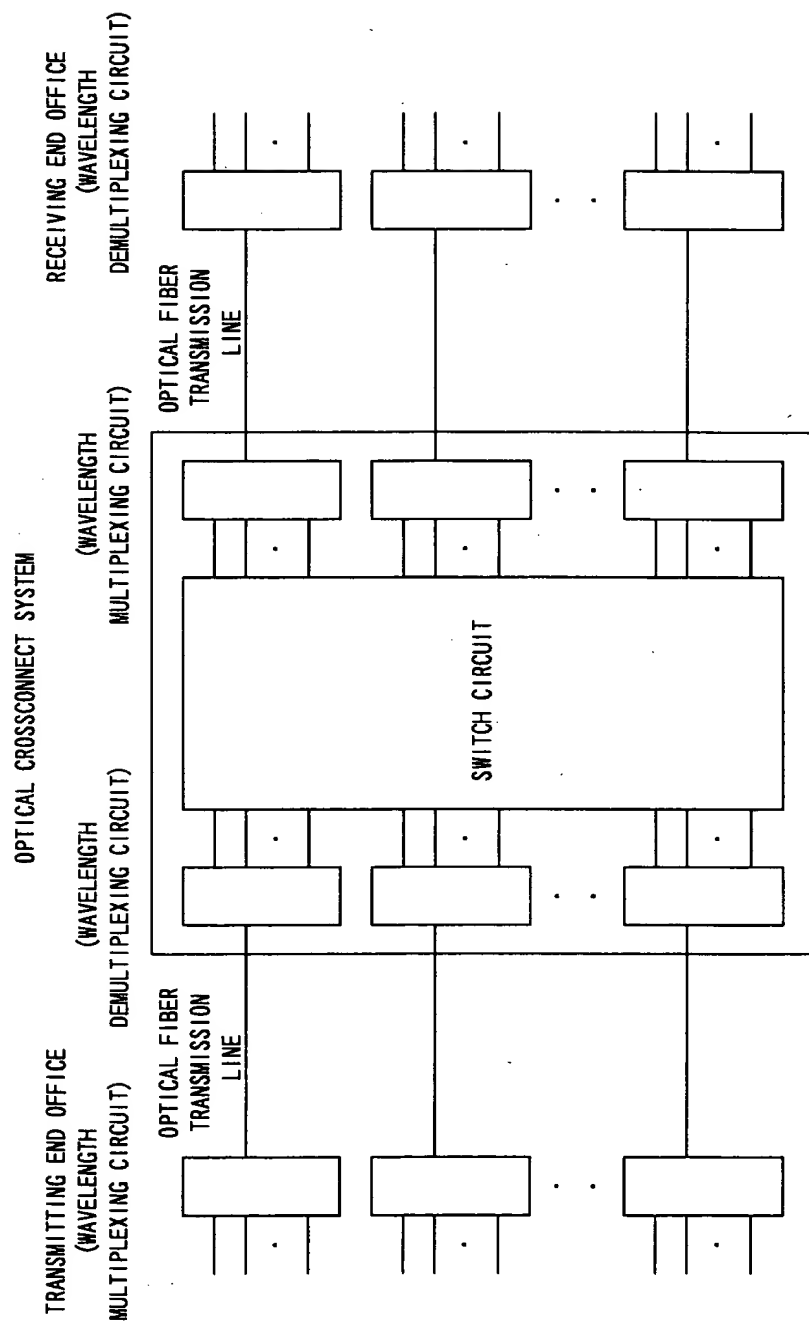


FIG. 3 PRIOR ART

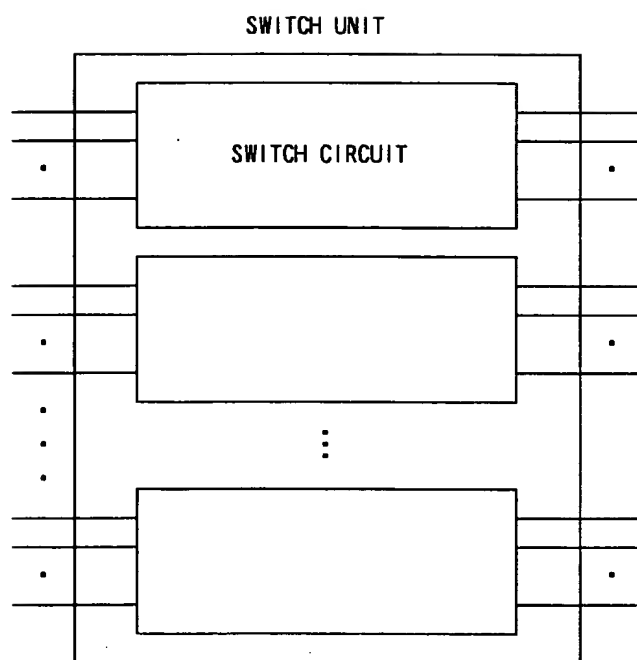
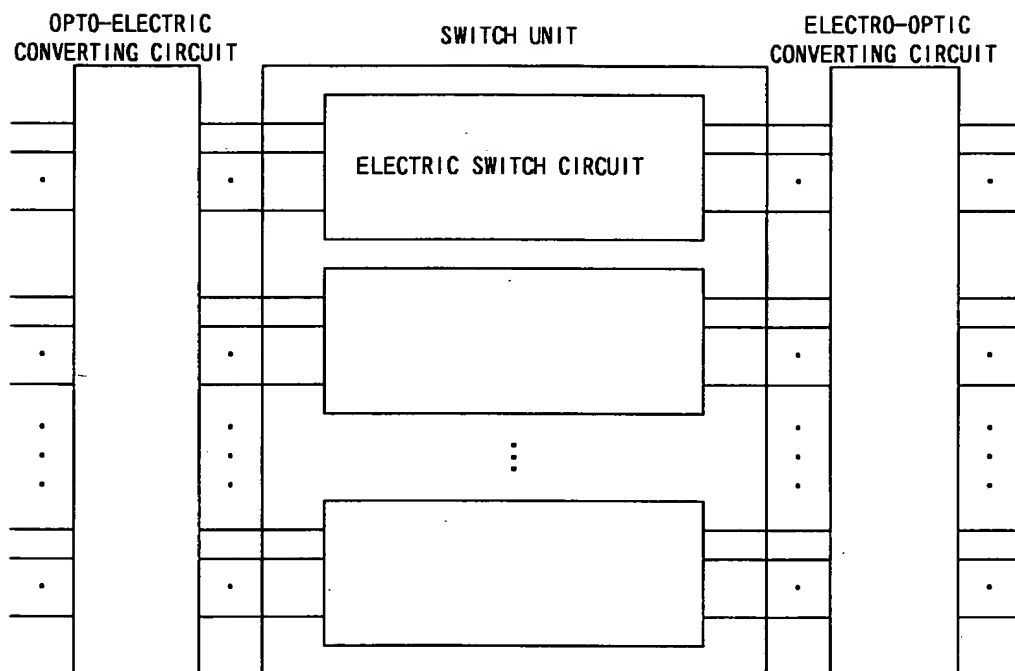
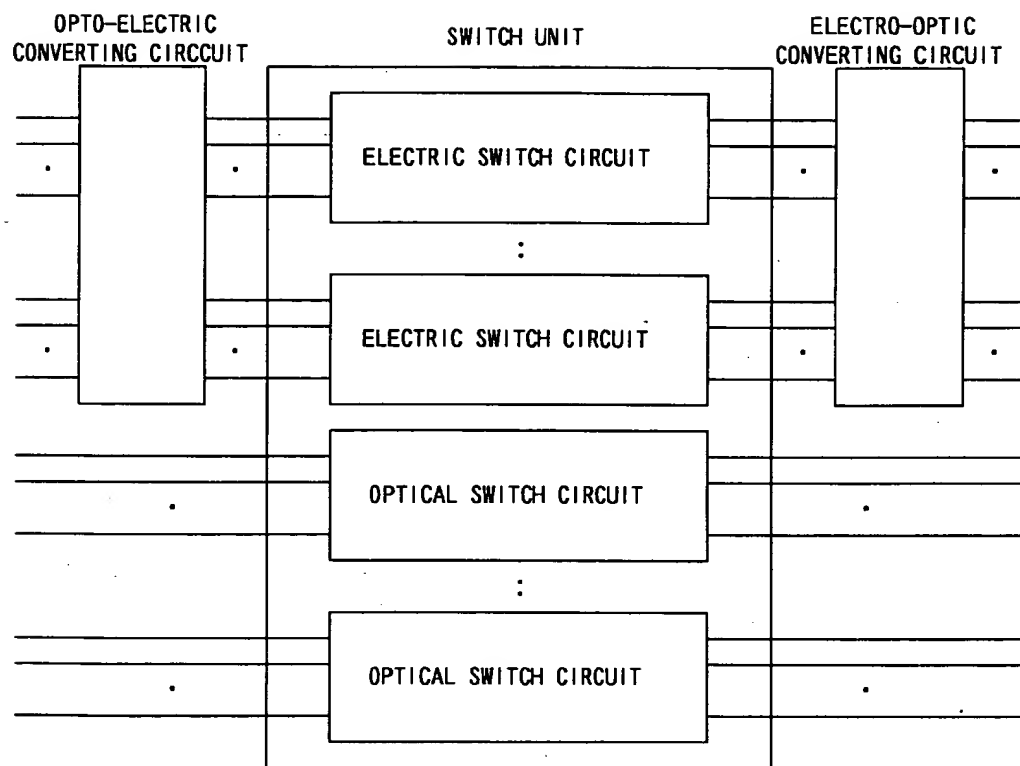


FIG. 4

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F I G. 5



F I G. 6

000001 220000 000001 220000

DocId:324460

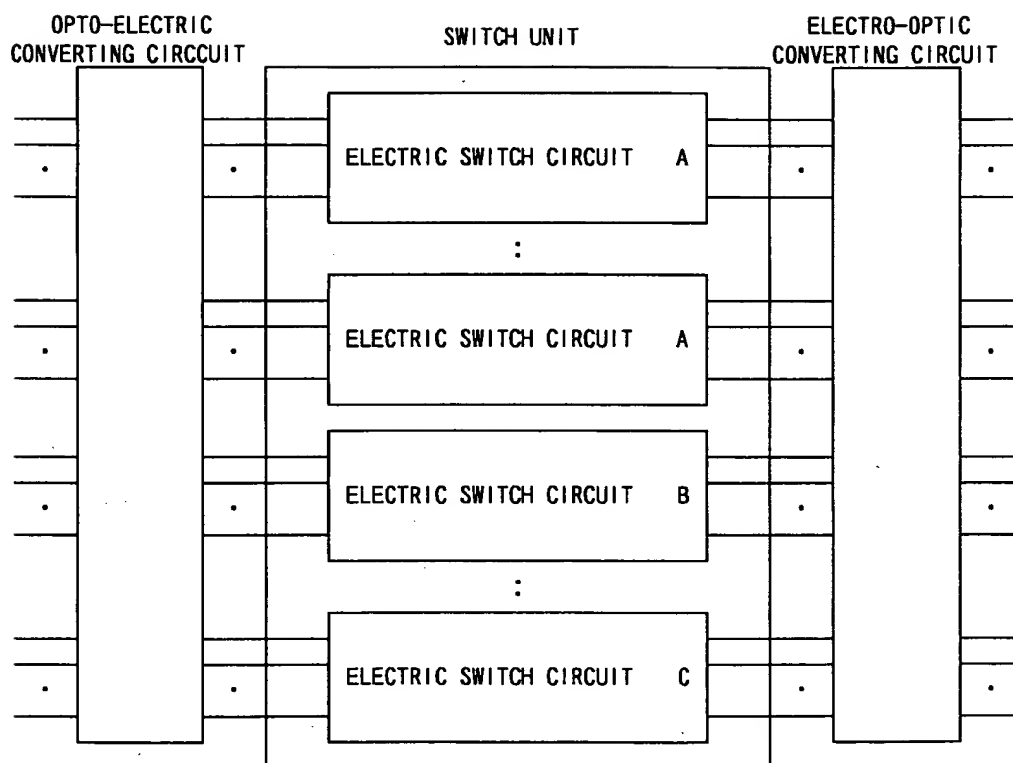
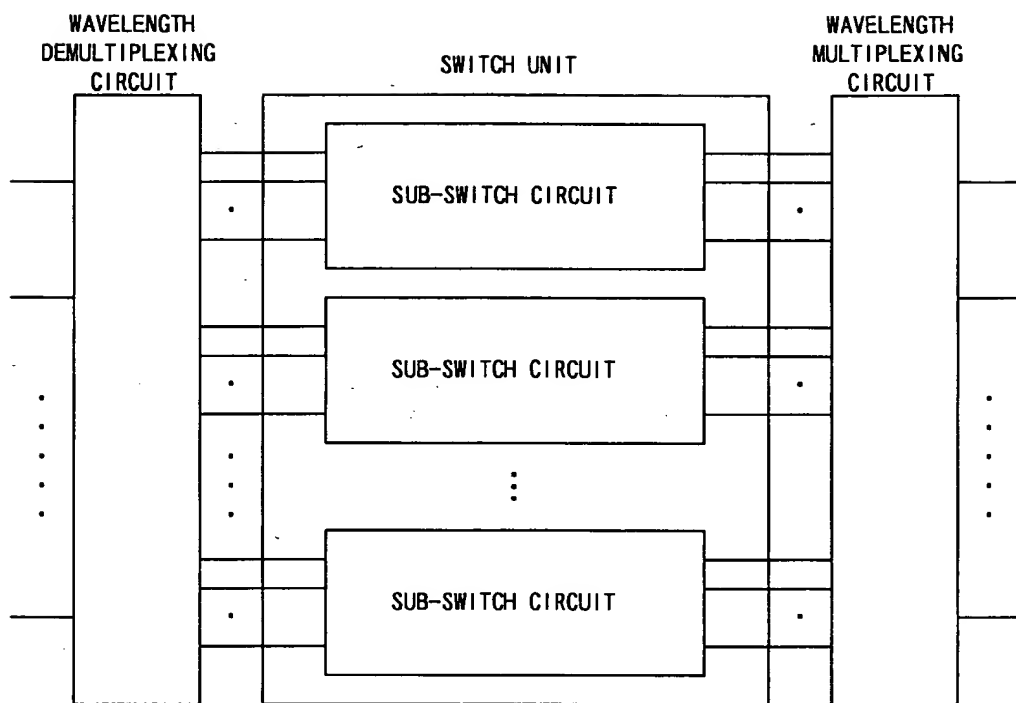
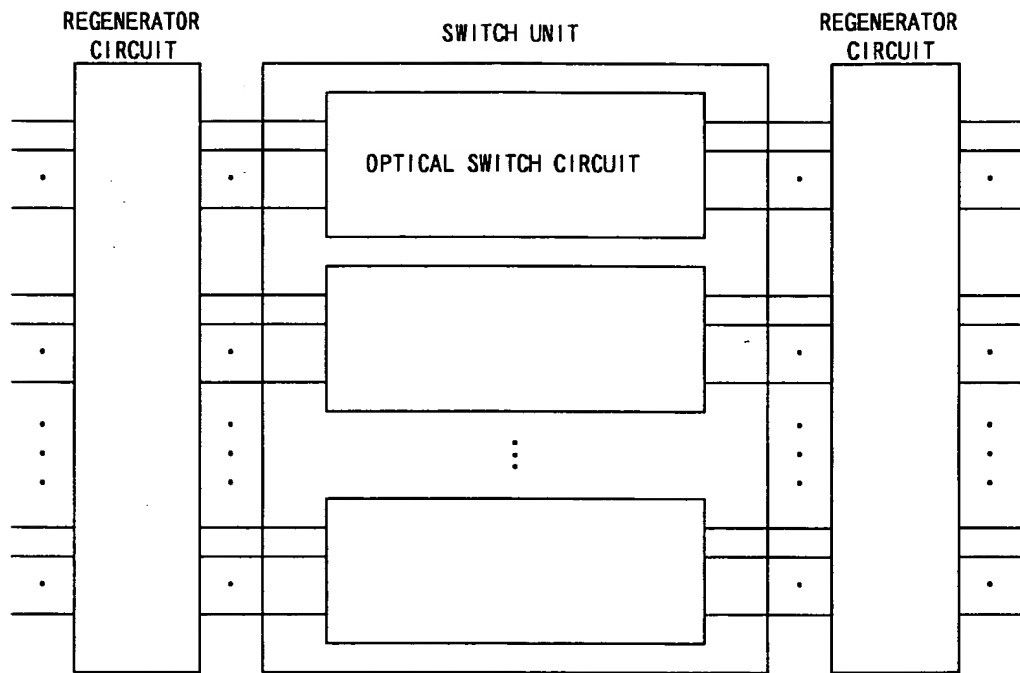


FIG. 7



F I G. 8

SECRET 32161400



F I G. 9

FIG. 10

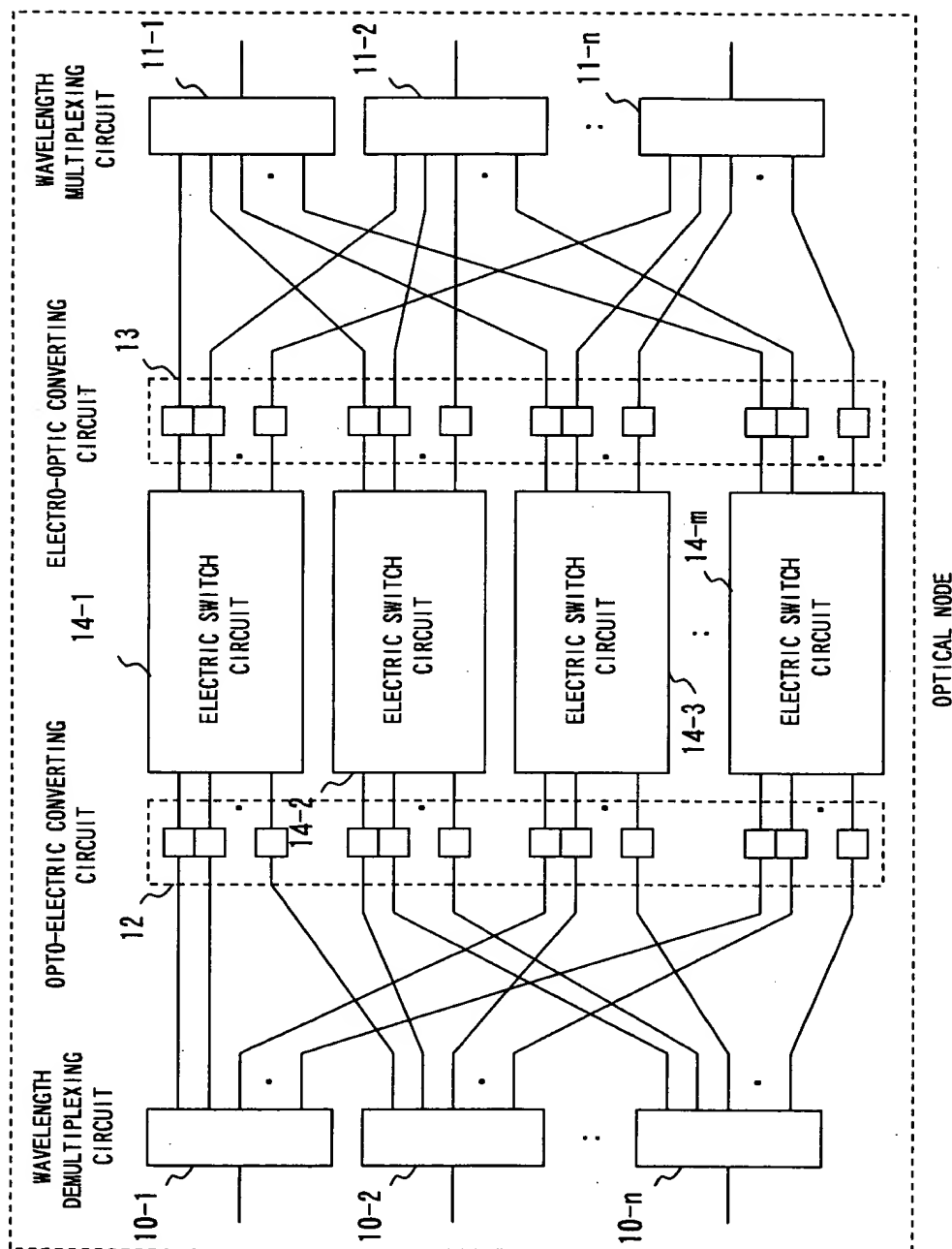
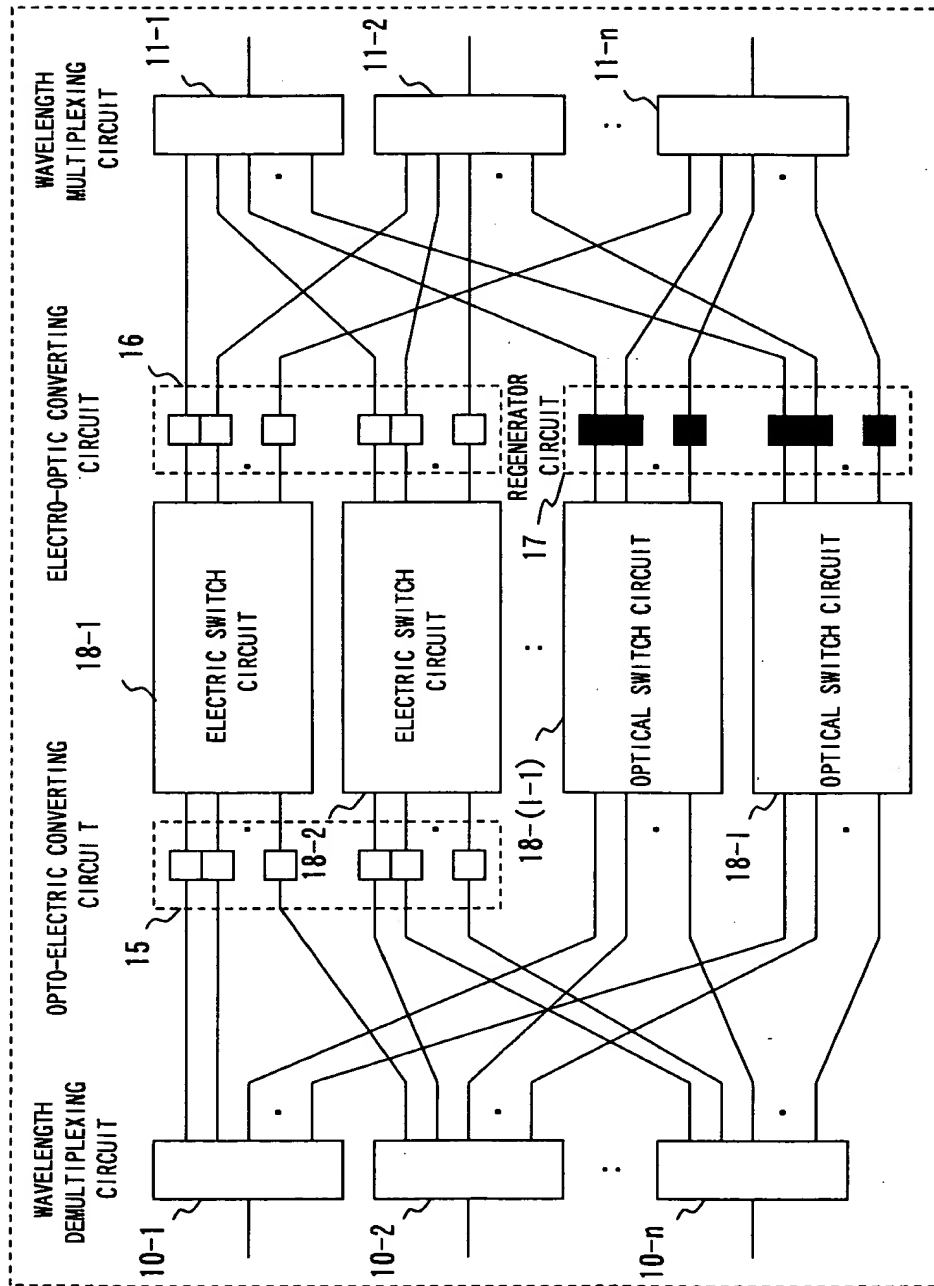


FIG. 11



OPTICAL NODE

FIG. 12

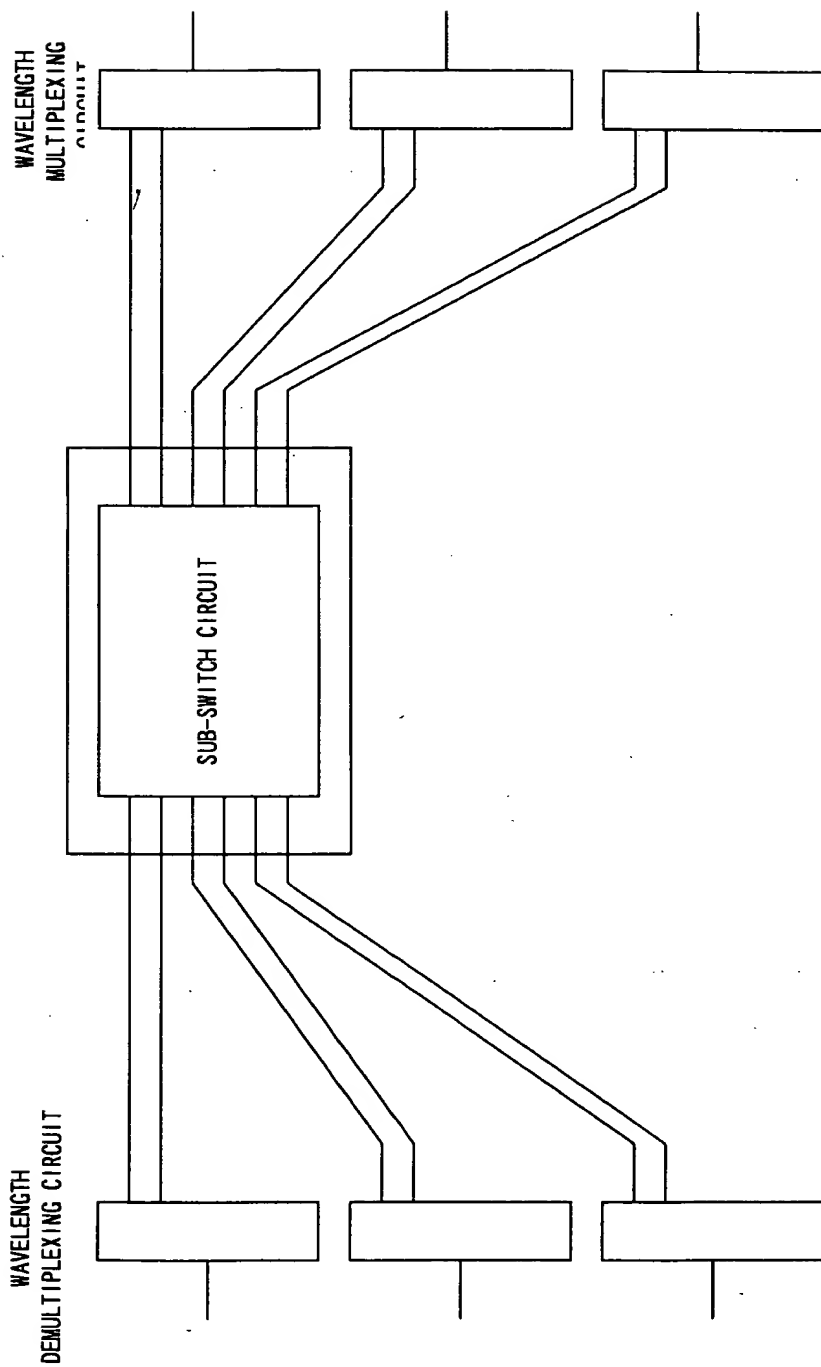


FIG. 13

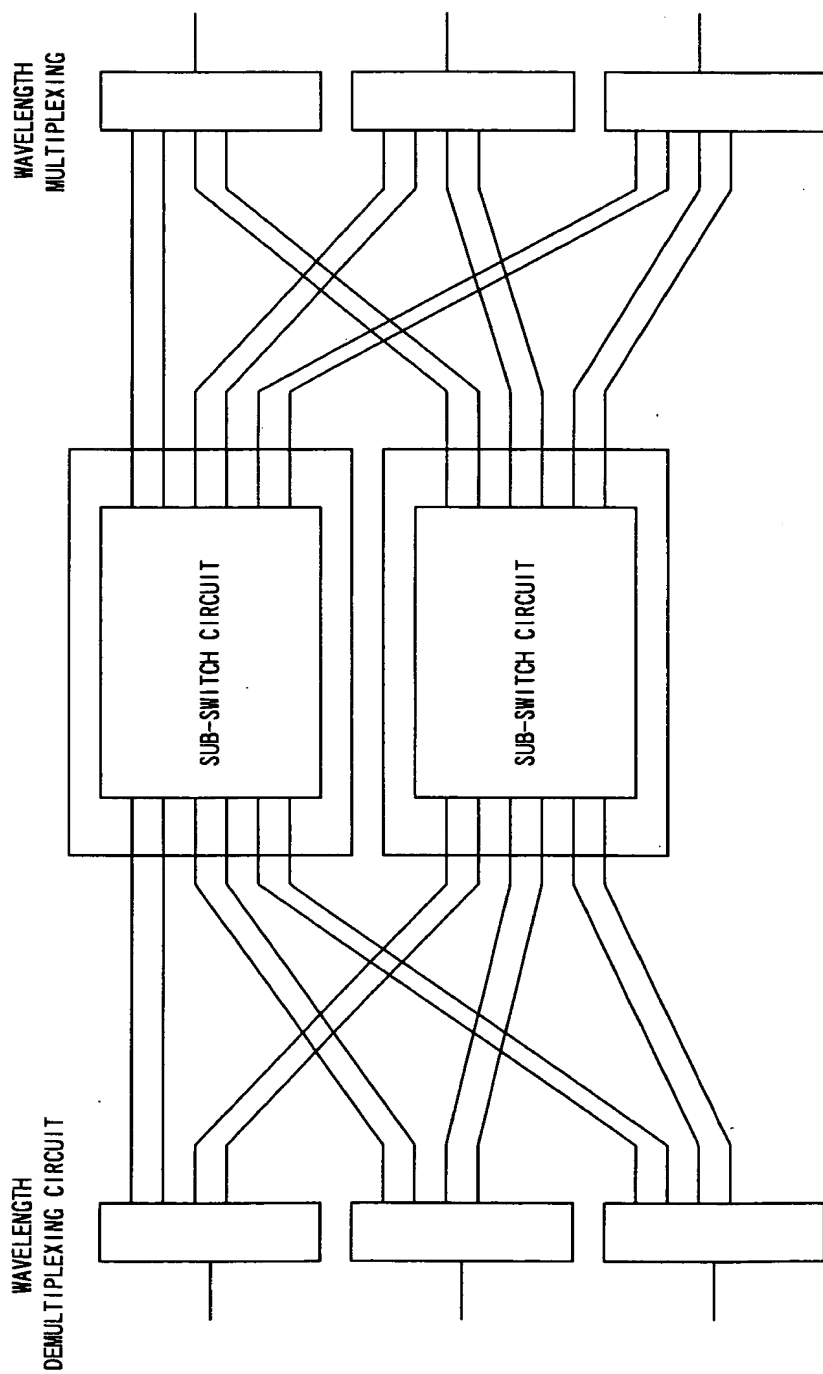


FIG. 14

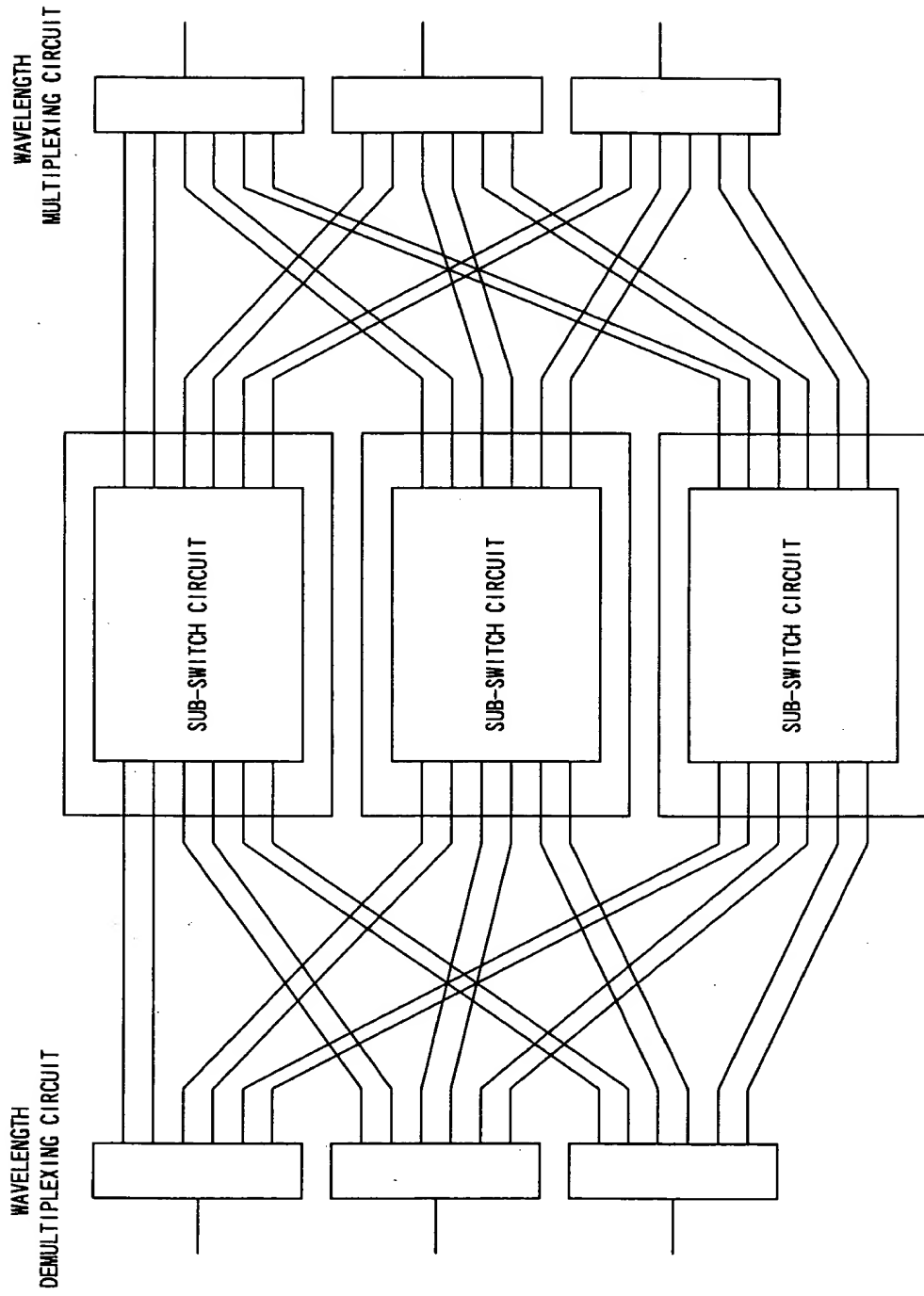
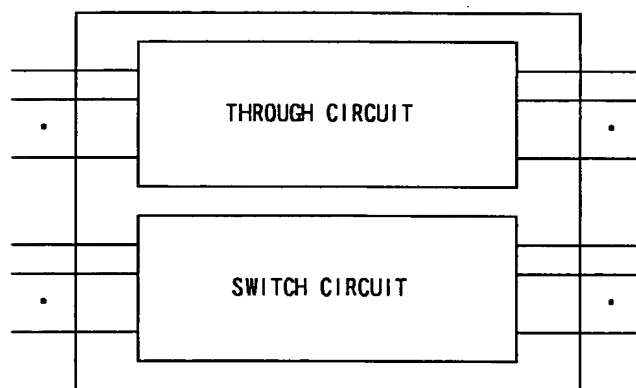


FIG. 15

000007 92000000



F I G. 1 6

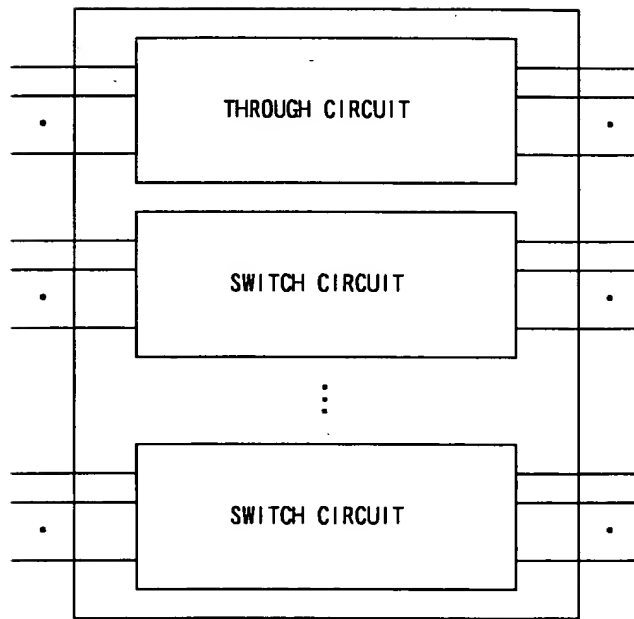


FIG. 17

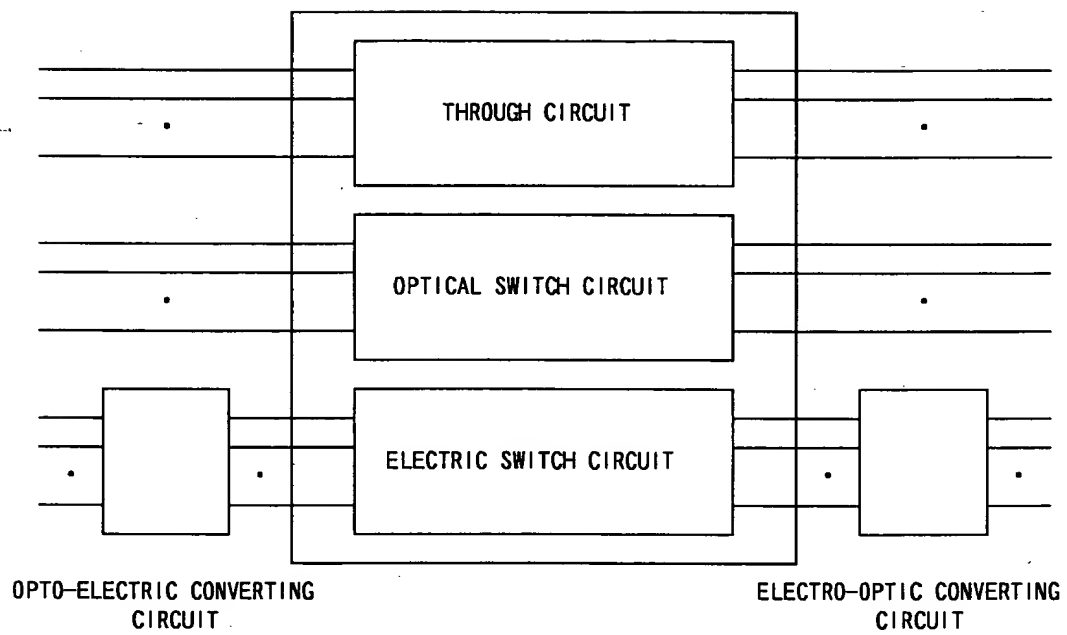


FIG. 18

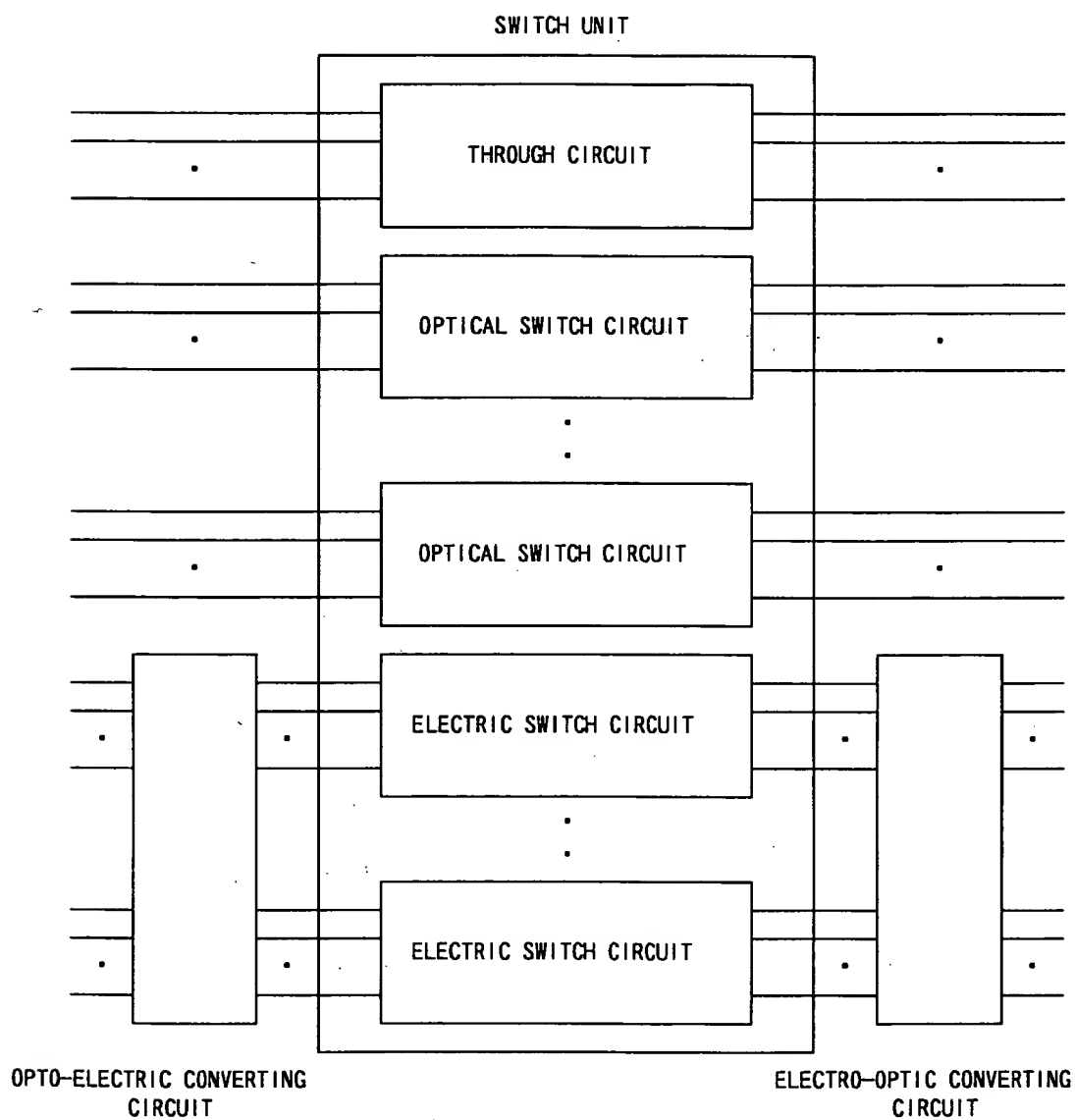
[illegible]

FIG. 19

The diagram illustrates the internal structure of a switch unit. At the top, a horizontal line is labeled "SWITCH UNIT". Below this, a central vertical column contains four rectangular blocks: "THROUGH CIRCUIT", "ELECTRIC SWITCH CIRCUIT A", "ELECTRIC SWITCH CIRCUIT B", and "ELECTRIC SWITCH CIRCUIT C". These blocks are connected to a horizontal line at the bottom labeled "ELECTRO-OPTIC CONVERTING CIRCUIT". To the left of the central column is a vertical rectangular block labeled "O-ELECTRIC CONVERTING CIRCUIT". To the right is another vertical rectangular block labeled "ELECTRO-OPTIC CONVERTING CIRCUIT". Horizontal lines connect the central blocks to the left and right blocks, indicating signal paths. Small dots are placed at the intersection points of these lines, representing connection points or components.

FIG. 20

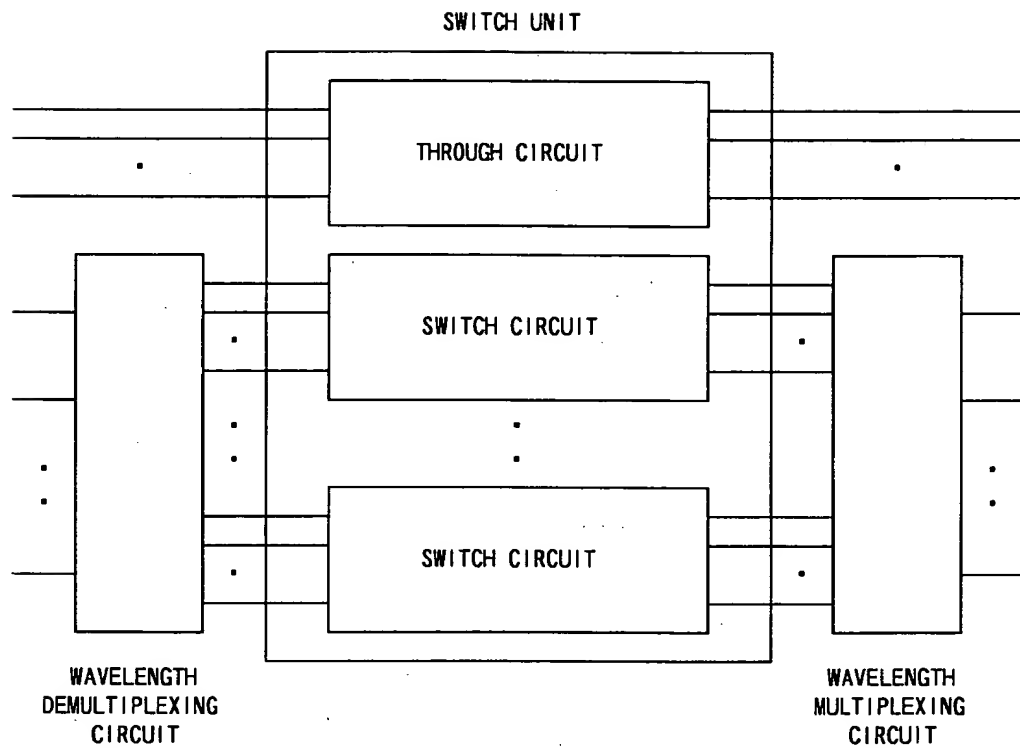
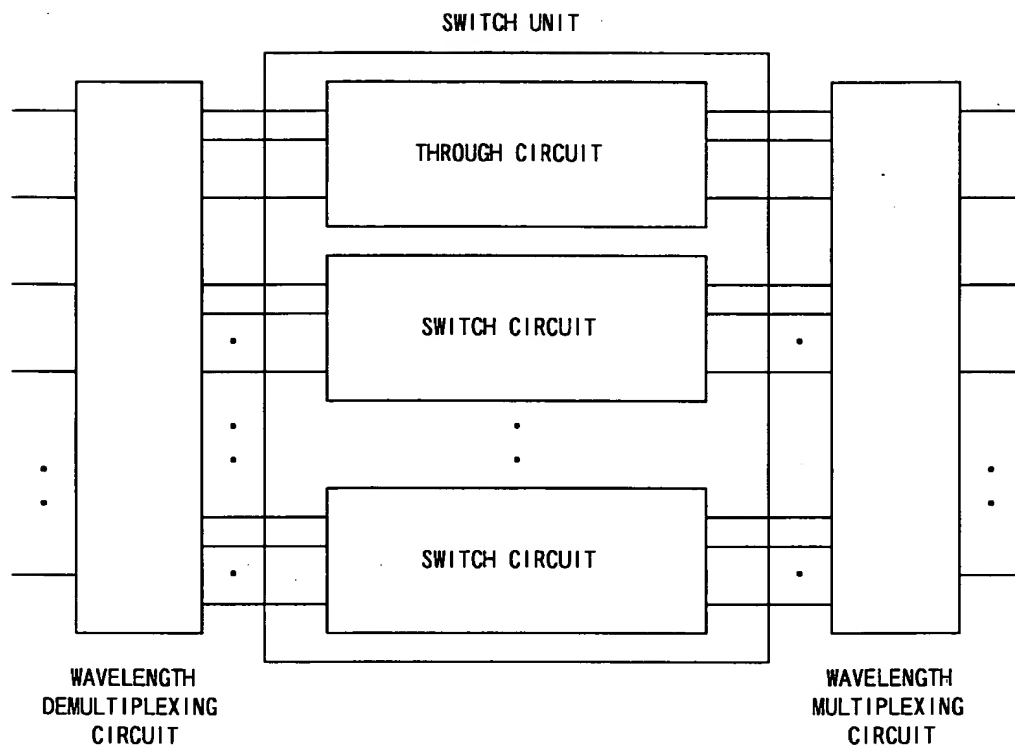


FIG. 21



F I G. 2 2

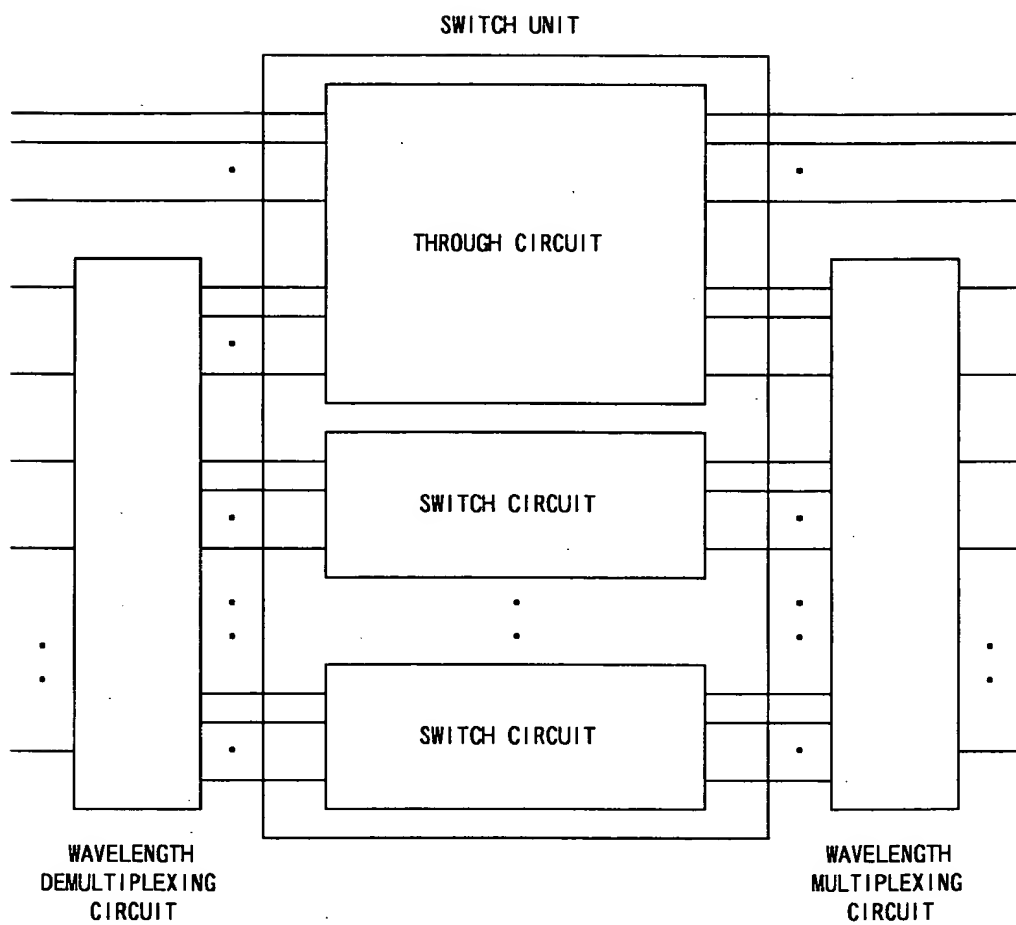


FIG. 23

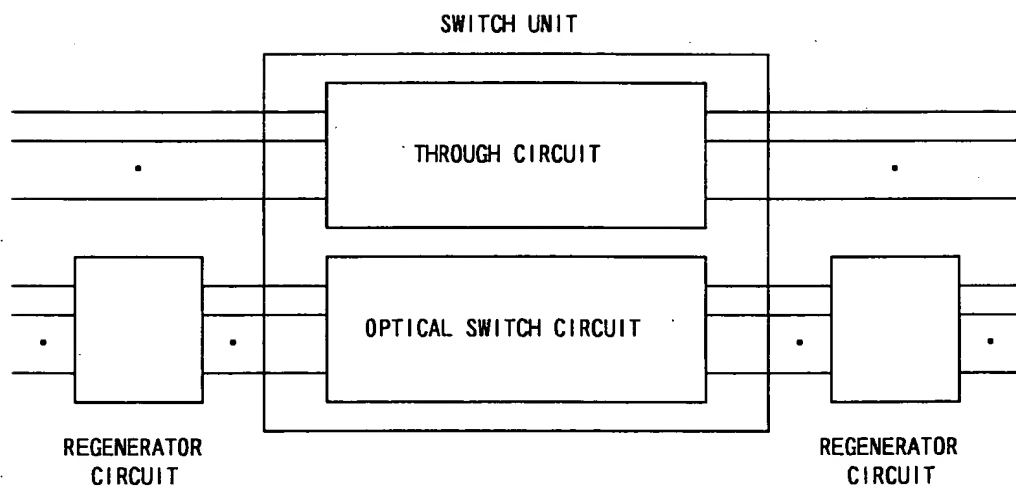
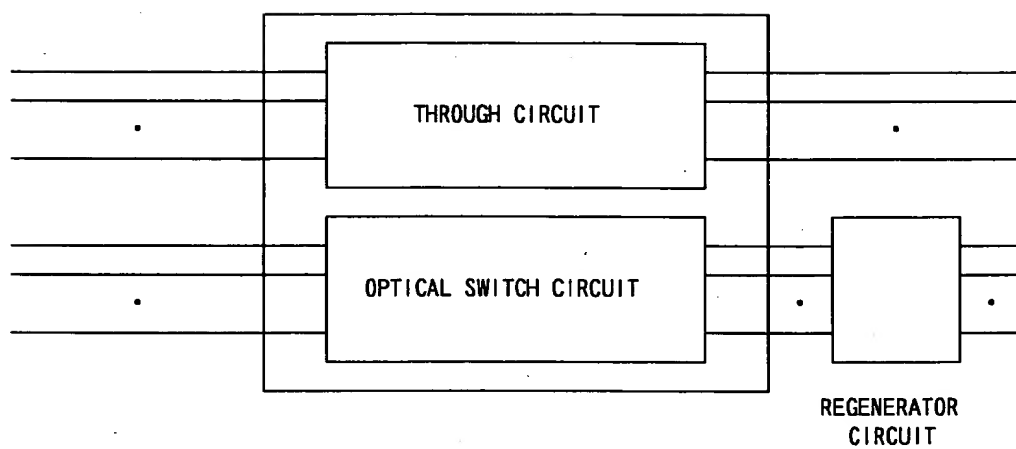


FIG. 24



F I G. 2 5

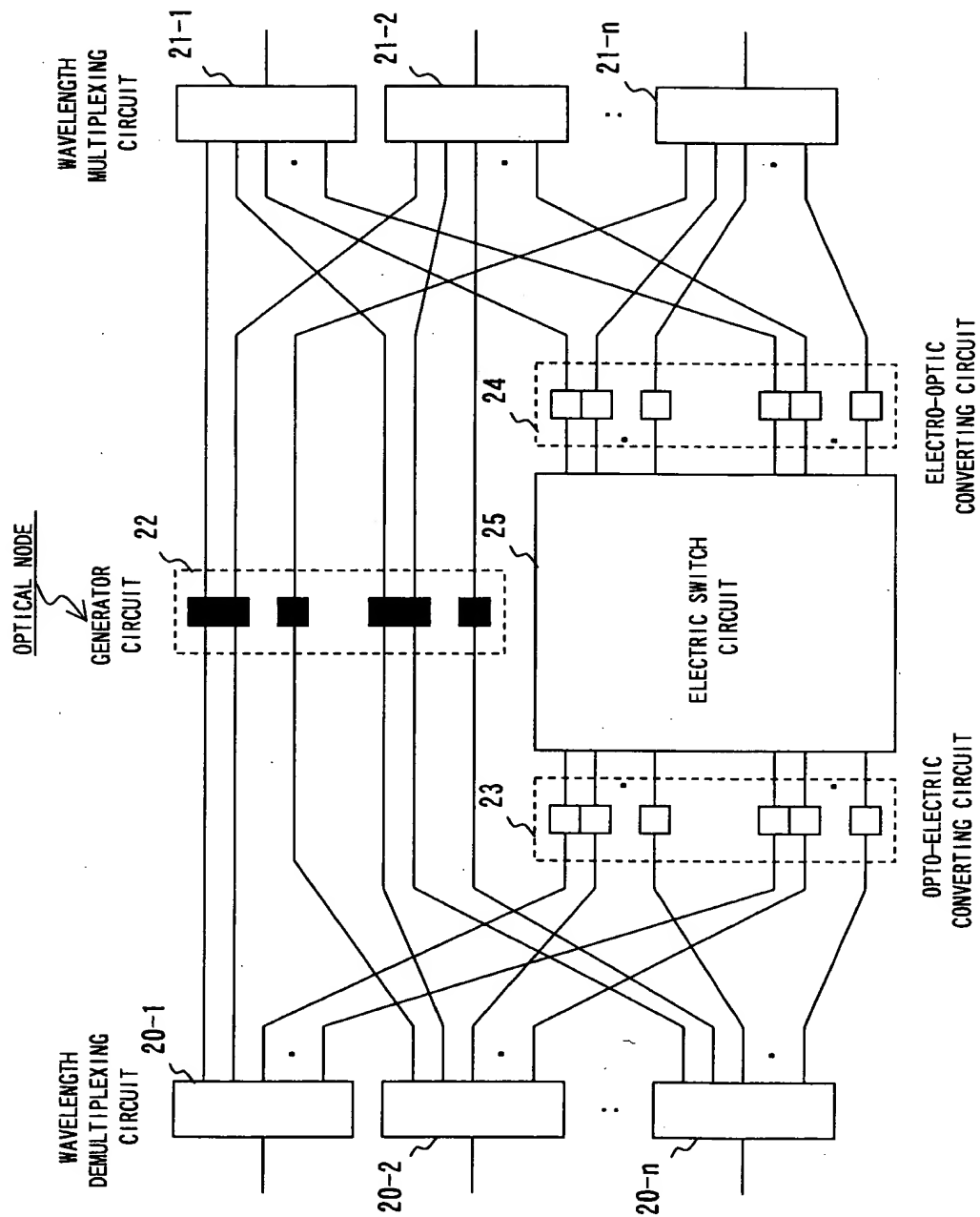


FIG. 26

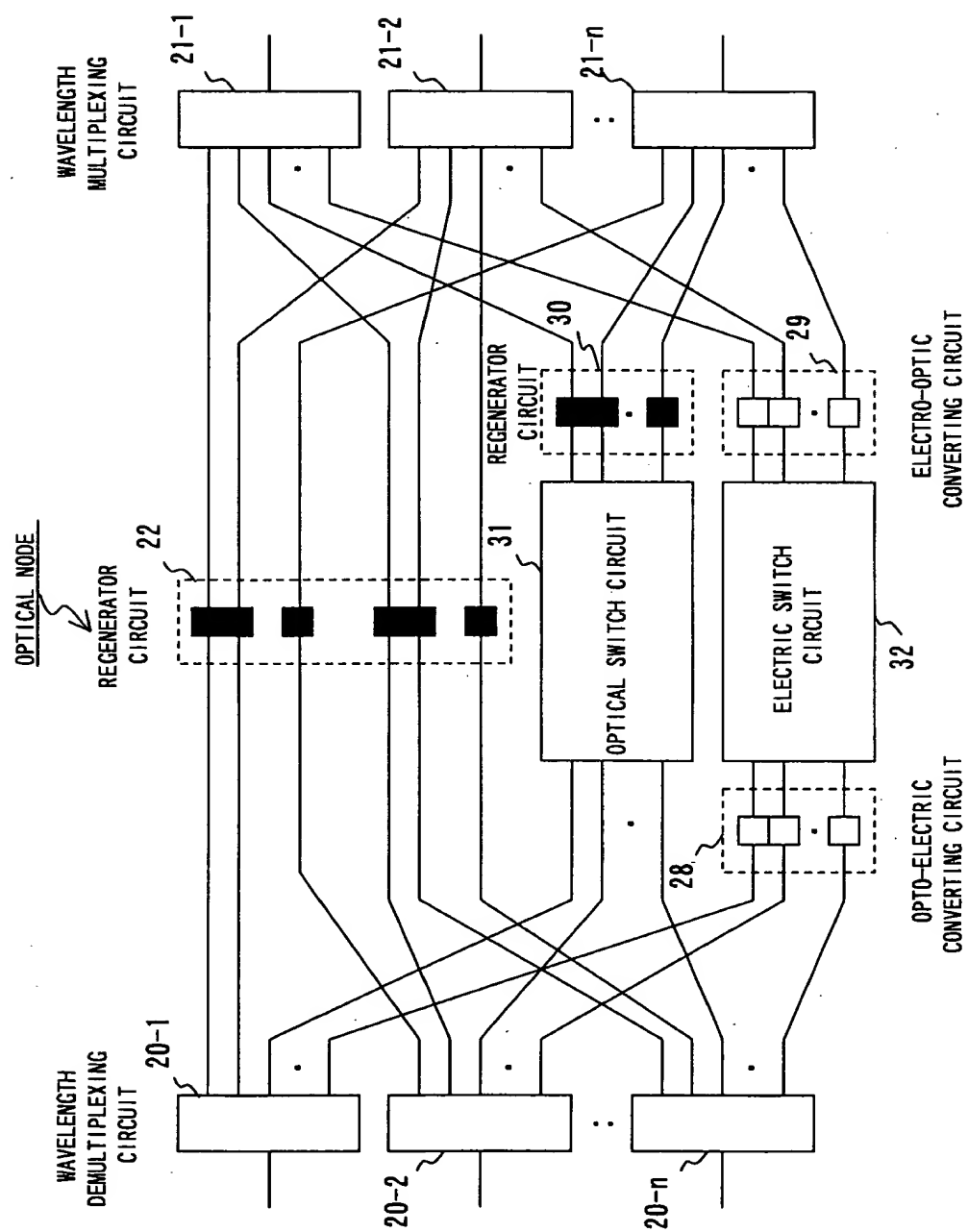


FIG. 27

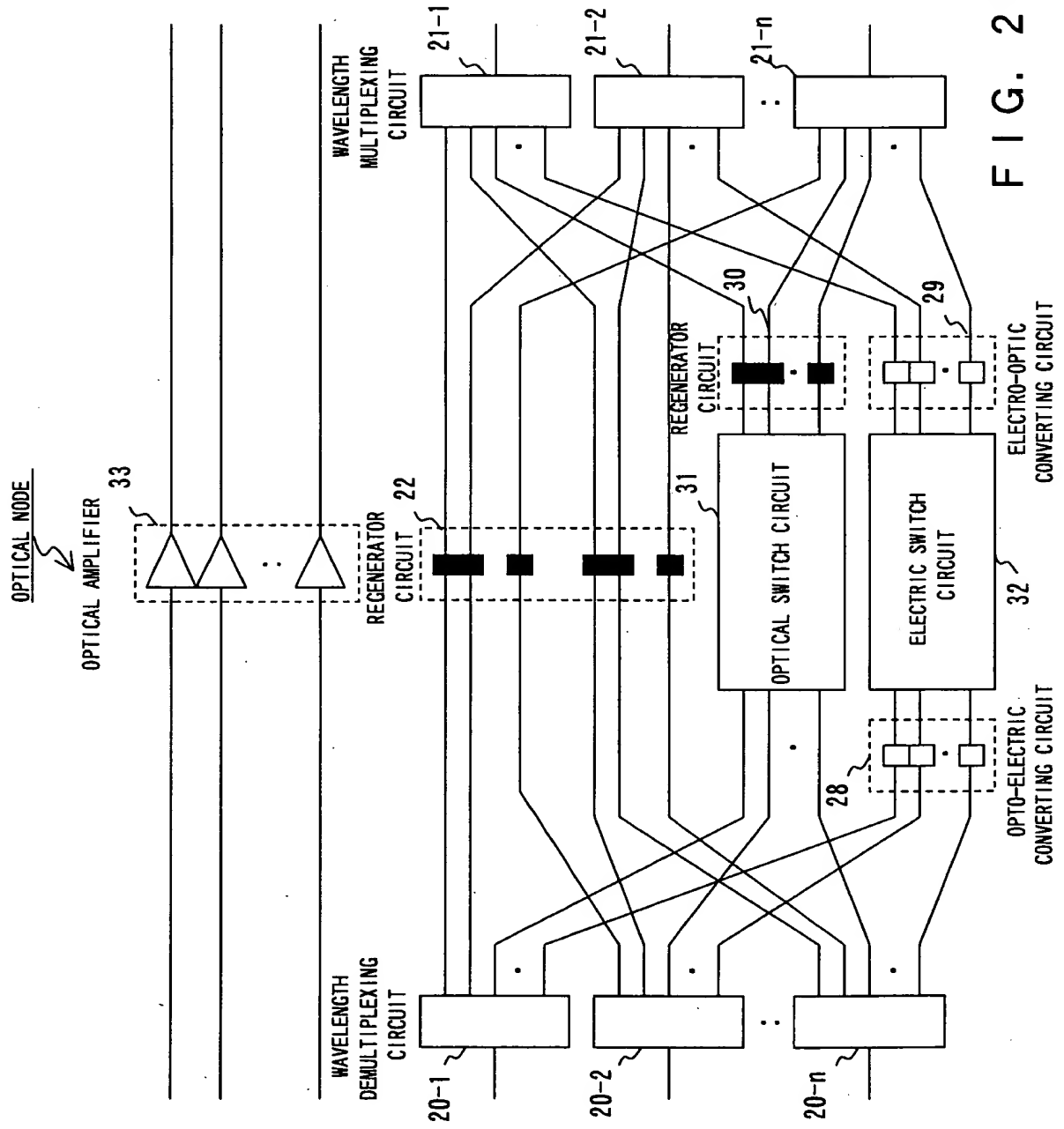


FIG. 28

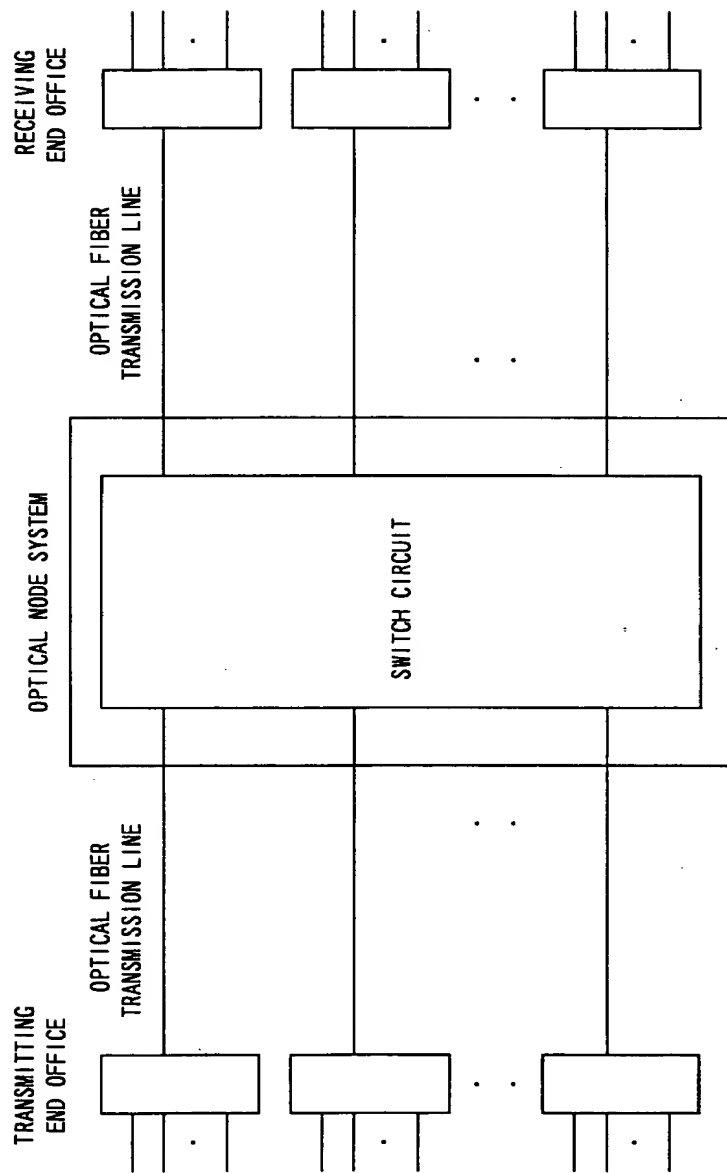
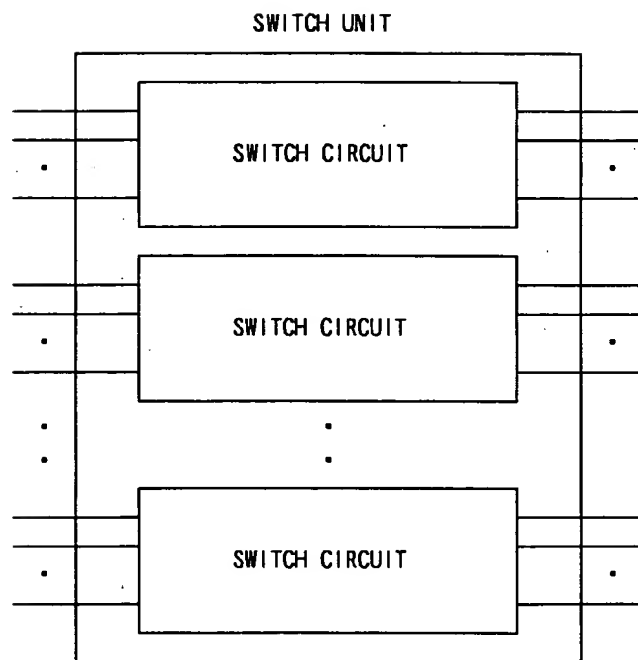
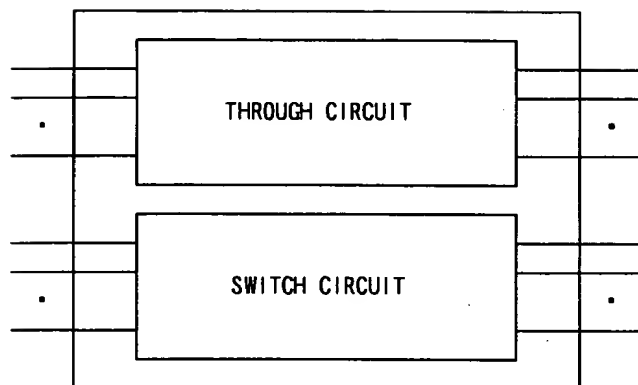


FIG. 29



F I G. 3 0

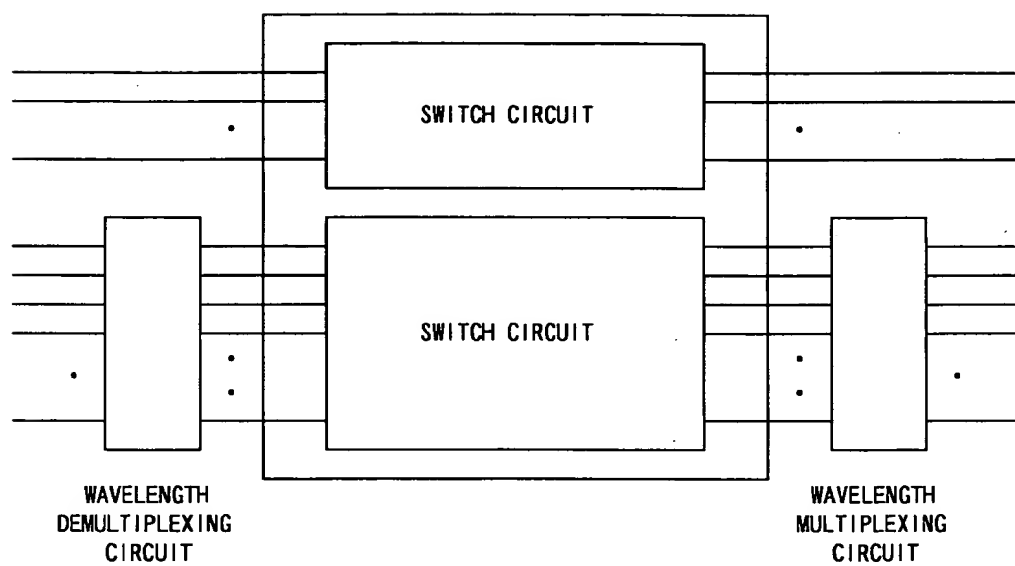
008227" sheet 2 of 2



F I G . 3 1

The diagram shows a 3x3 grid of circuit components. The top row contains a 'THROUGH CIRCUIT'. The middle row contains a 'SWITCH CIRCUIT'. The bottom row contains a 'SWITCH CIRCUIT'. Each component is represented by a rectangle with its name inside. The grid is defined by horizontal and vertical lines, with small dots at the intersections of the lines.

FIG. 32



F I G . 3 3

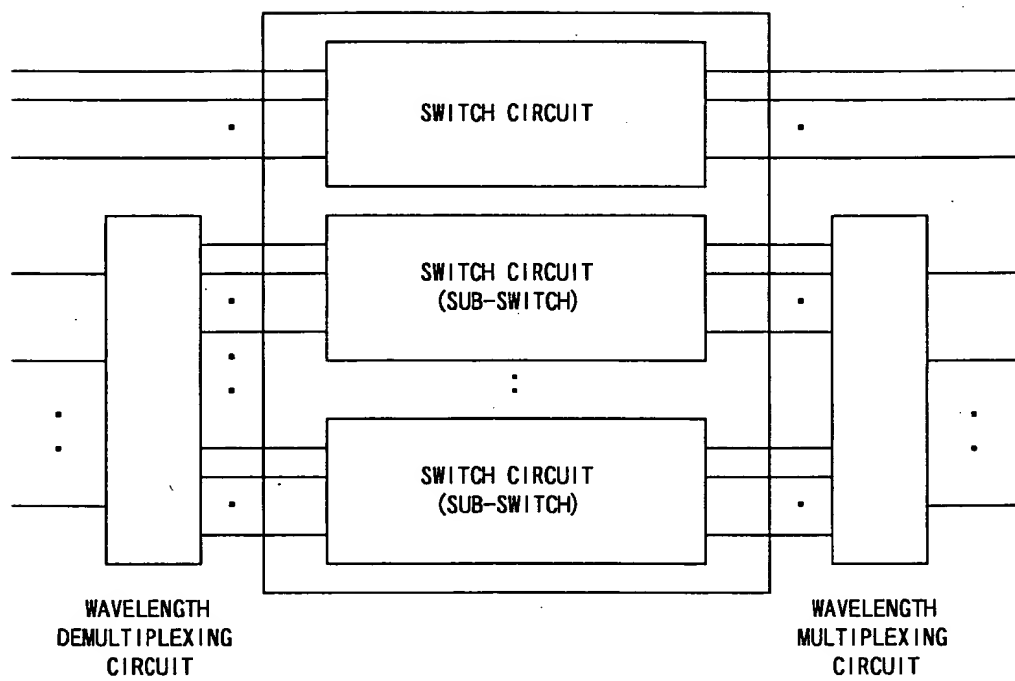


FIG. 34

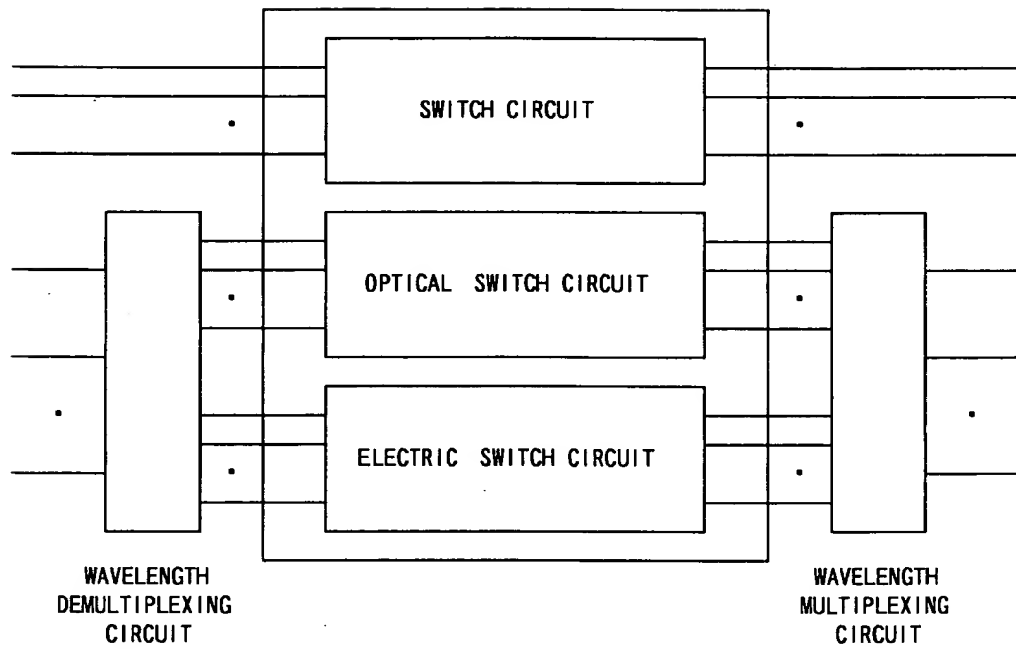
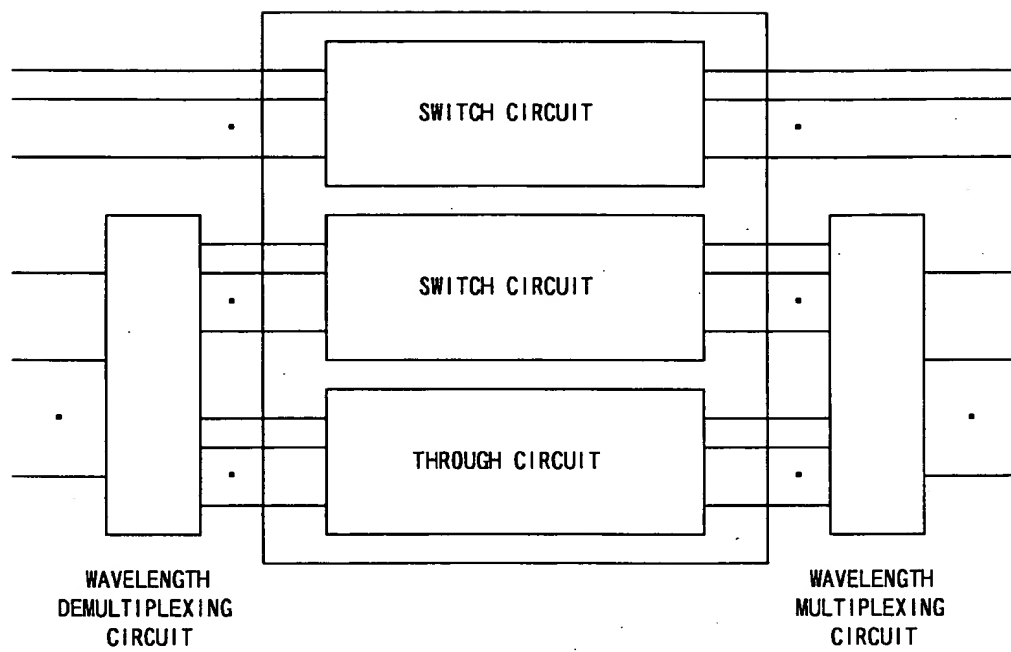
$$\begin{array}{ccccccc} \left\{ \begin{array}{c} \{f^{(2)}_{11}\} \\ \{f^{(2)}_{12}\} \\ \vdots \\ \{f^{(2)}_{1n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{21}\} \\ \{f^{(2)}_{22}\} \\ \vdots \\ \{f^{(2)}_{2n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{31}\} \\ \{f^{(2)}_{32}\} \\ \vdots \\ \{f^{(2)}_{3n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{41}\} \\ \{f^{(2)}_{42}\} \\ \vdots \\ \{f^{(2)}_{4n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{51}\} \\ \{f^{(2)}_{52}\} \\ \vdots \\ \{f^{(2)}_{5n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{61}\} \\ \{f^{(2)}_{62}\} \\ \vdots \\ \{f^{(2)}_{6n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{71}\} \\ \{f^{(2)}_{72}\} \\ \vdots \\ \{f^{(2)}_{7n}\} \end{array} \right\} \\ \left\{ \begin{array}{c} \{f^{(2)}_{11}\} \\ \{f^{(2)}_{12}\} \\ \vdots \\ \{f^{(2)}_{1n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{21}\} \\ \{f^{(2)}_{22}\} \\ \vdots \\ \{f^{(2)}_{2n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{31}\} \\ \{f^{(2)}_{32}\} \\ \vdots \\ \{f^{(2)}_{3n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{41}\} \\ \{f^{(2)}_{42}\} \\ \vdots \\ \{f^{(2)}_{4n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{51}\} \\ \{f^{(2)}_{52}\} \\ \vdots \\ \{f^{(2)}_{5n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{61}\} \\ \{f^{(2)}_{62}\} \\ \vdots \\ \{f^{(2)}_{6n}\} \end{array} \right\} & \left\{ \begin{array}{c} \{f^{(2)}_{71}\} \\ \{f^{(2)}_{72}\} \\ \vdots \\ \{f^{(2)}_{7n}\} \end{array} \right\} \end{array}$$


FIG. 35



F I G. 3 6

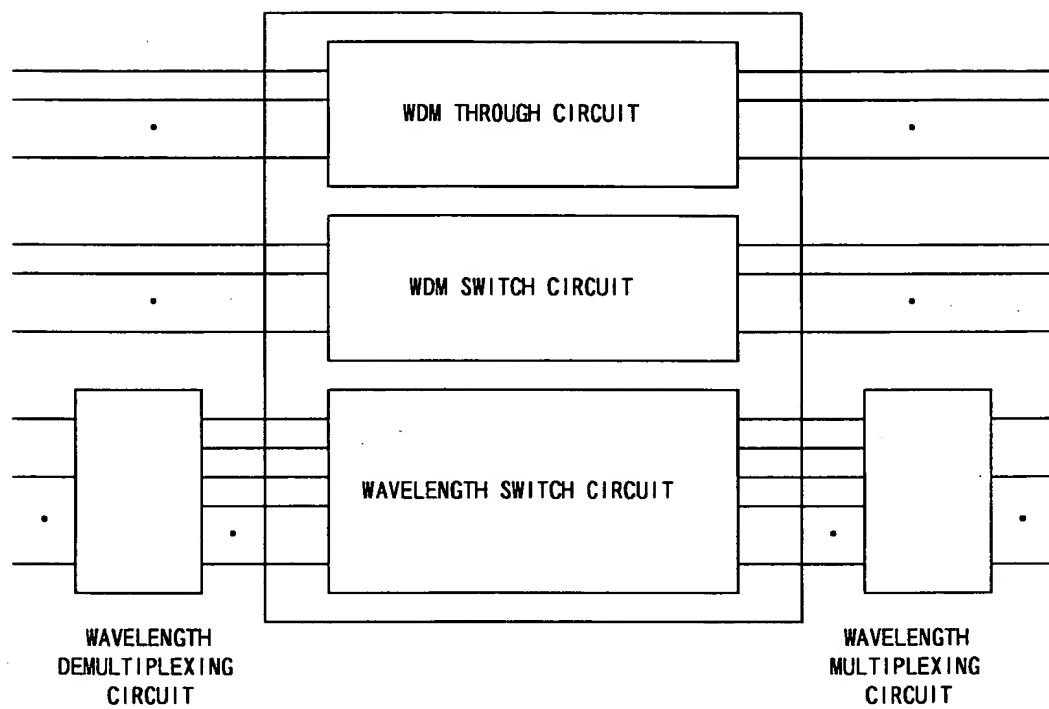


FIG. 37

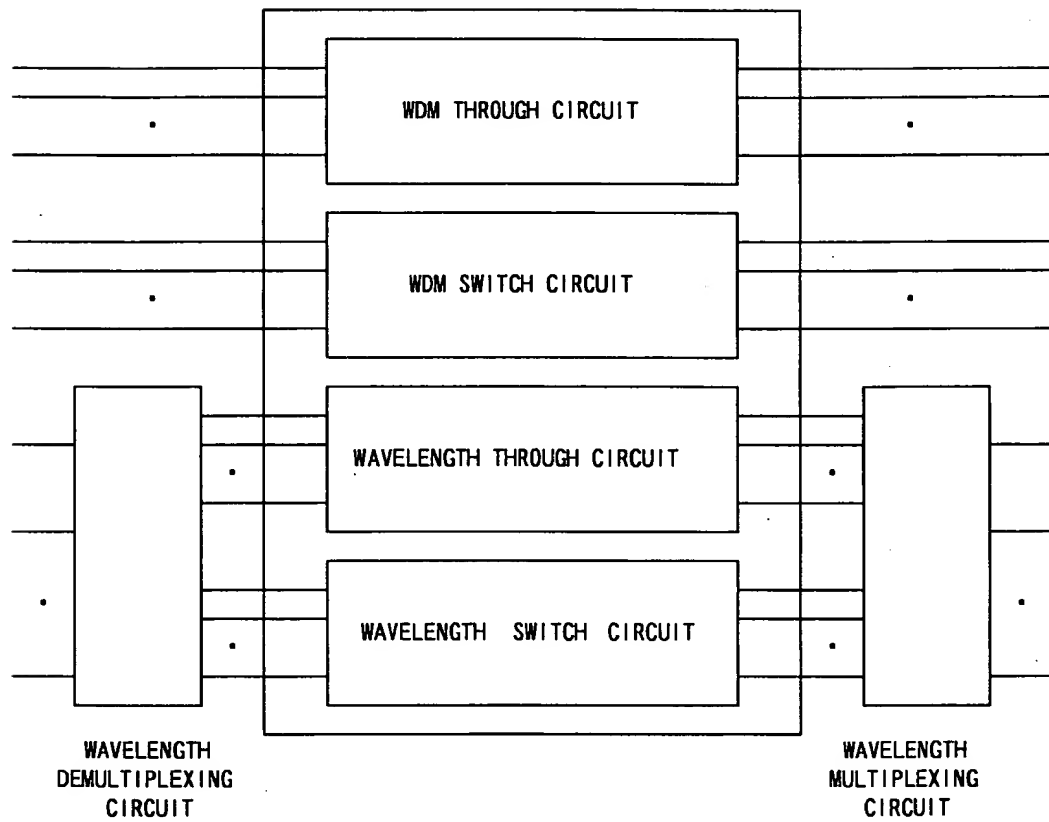


FIG. 38

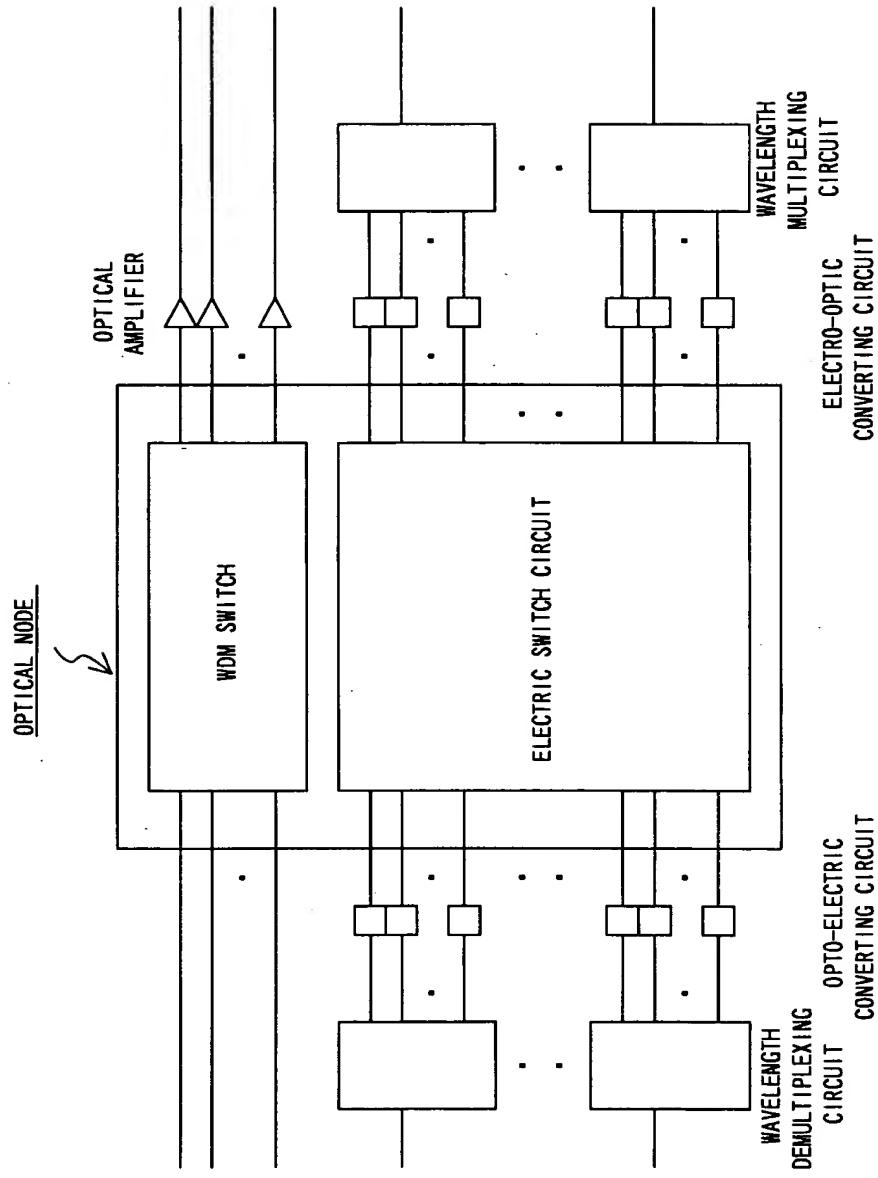


FIG. 39

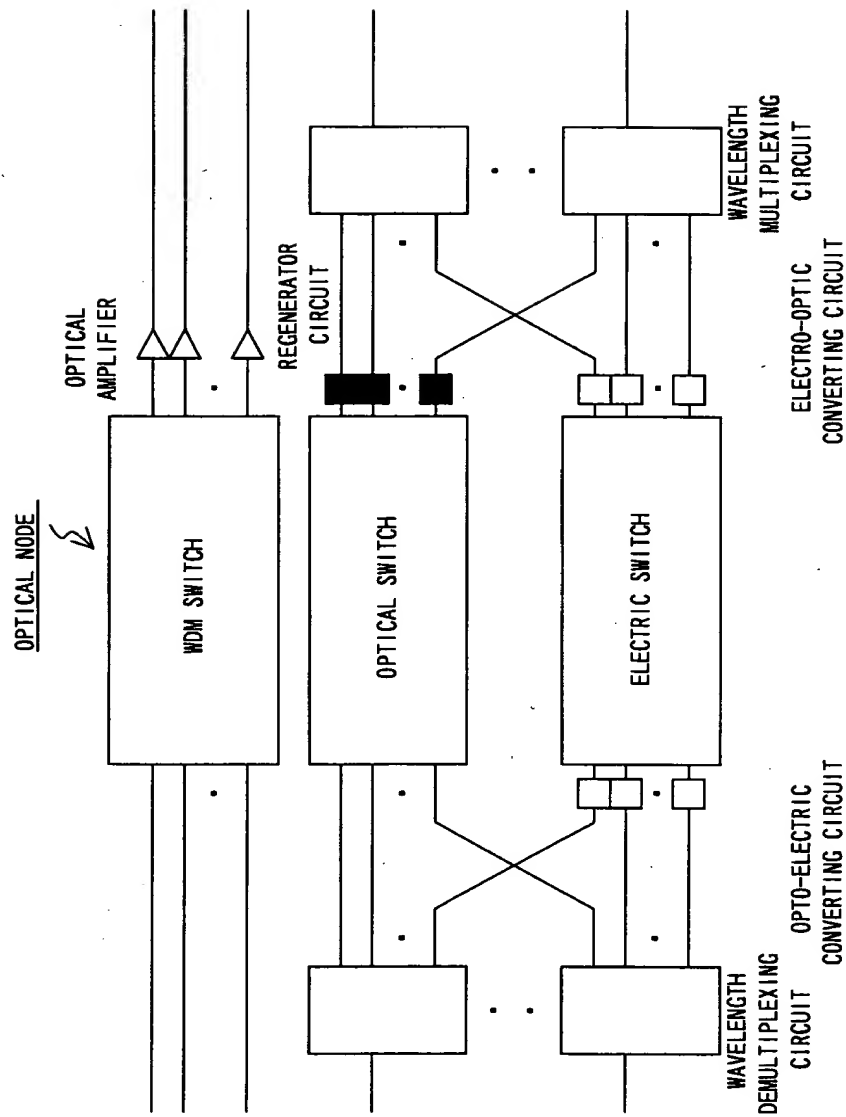


FIG. 40

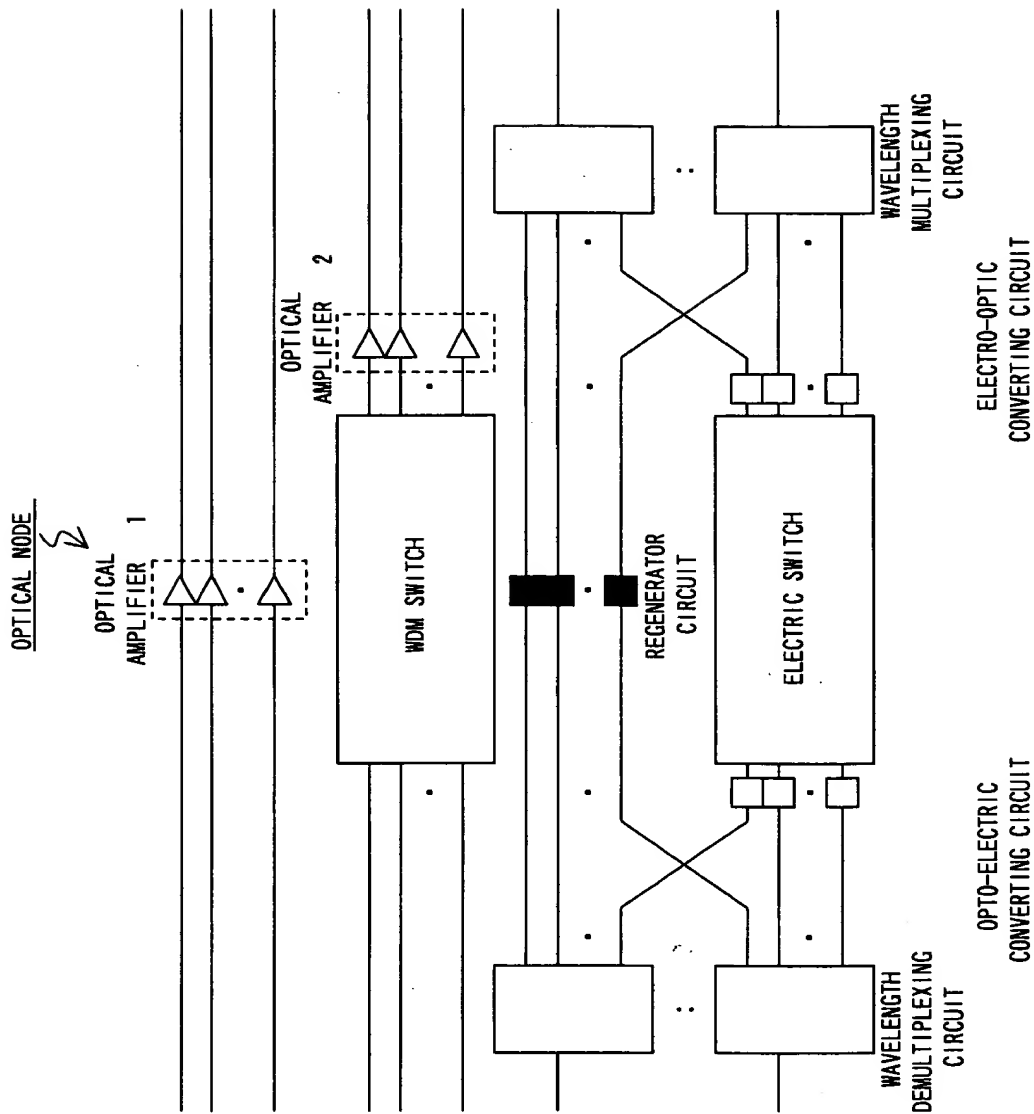


FIG. 41

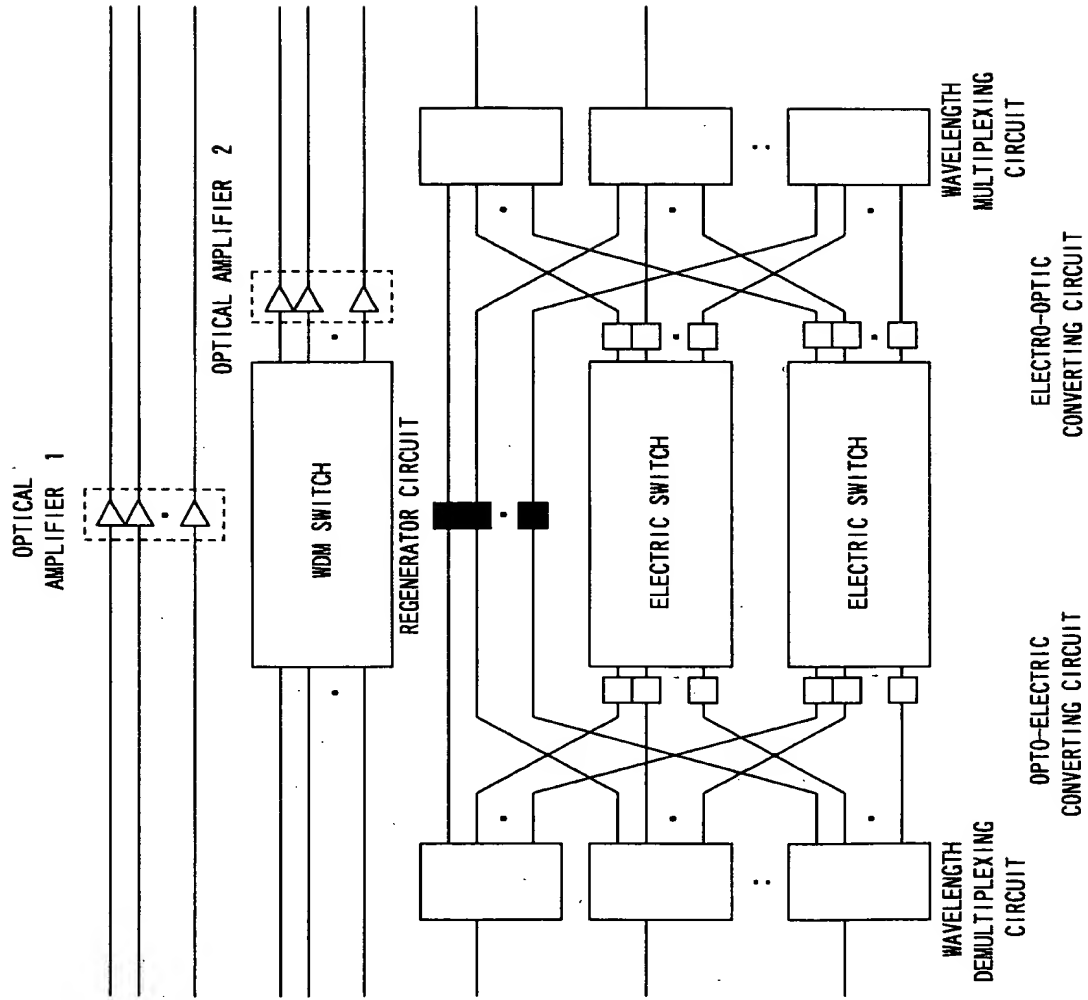
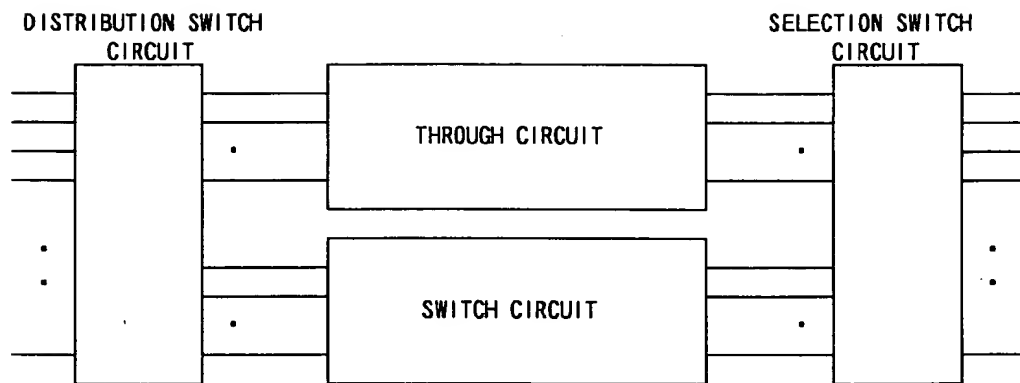


FIG. 42



F I G. 4 3

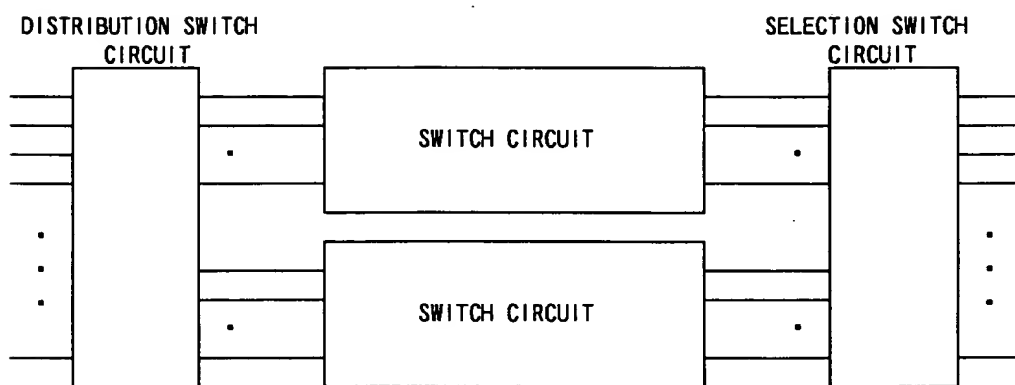
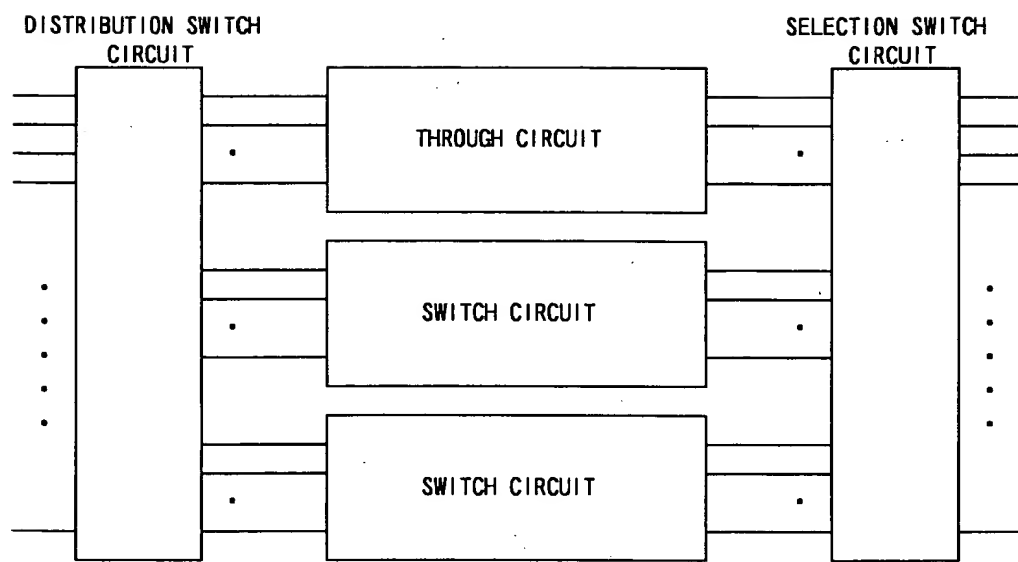
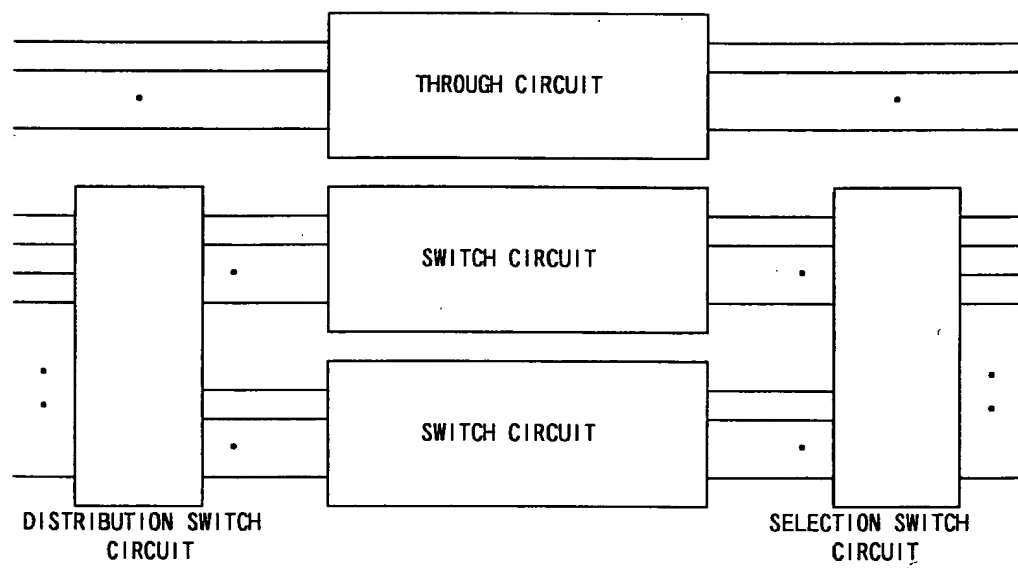
[illegible]

FIG. 44



F I G . 4 5

000001" 3044260



F I G. 4 6

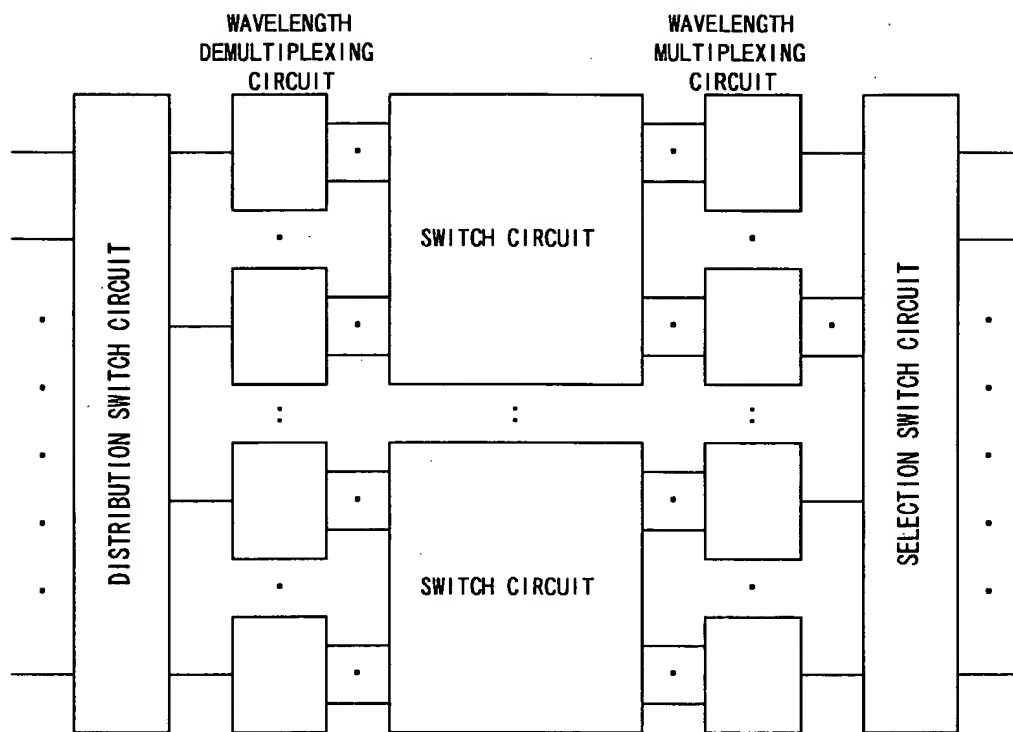


FIG. 47

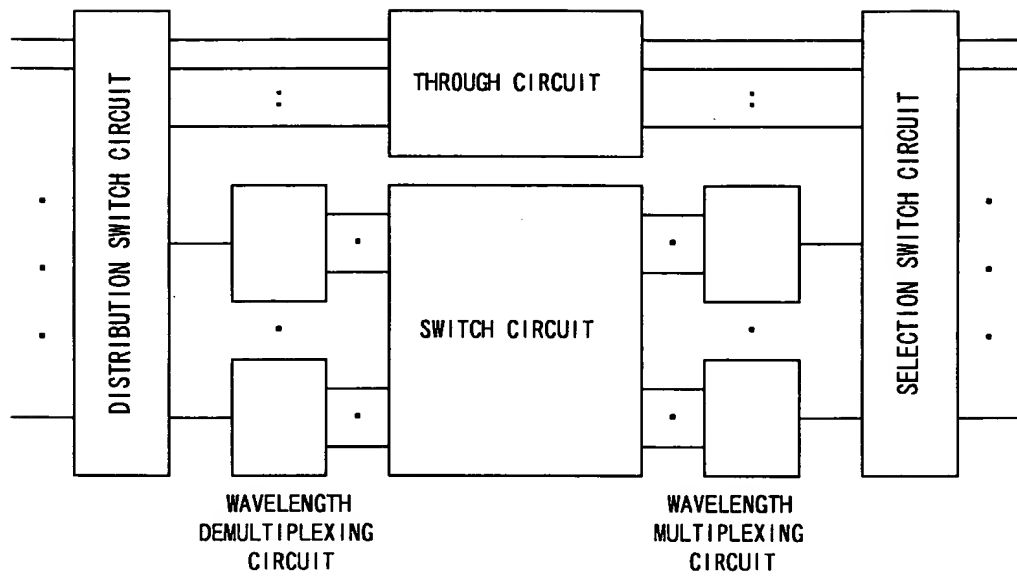


FIG. 48

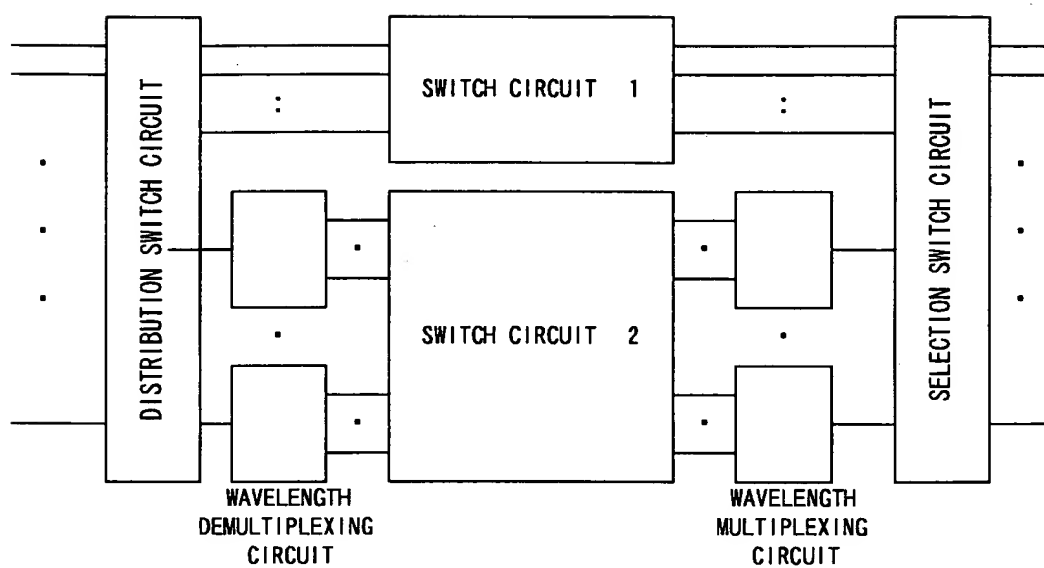


FIG. 49

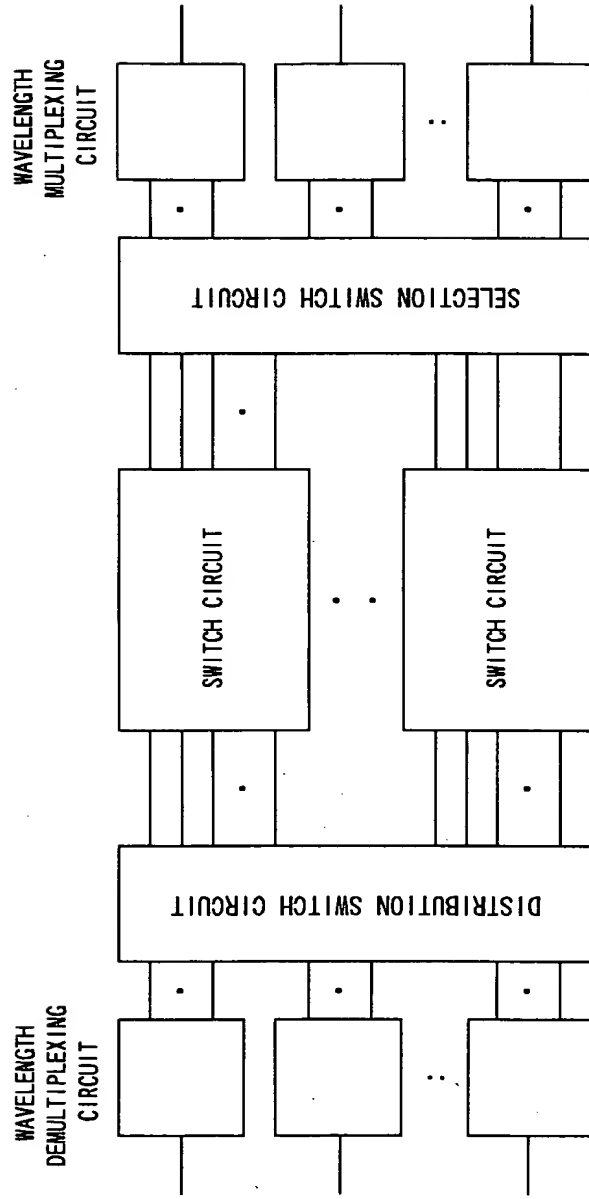


FIG. 50

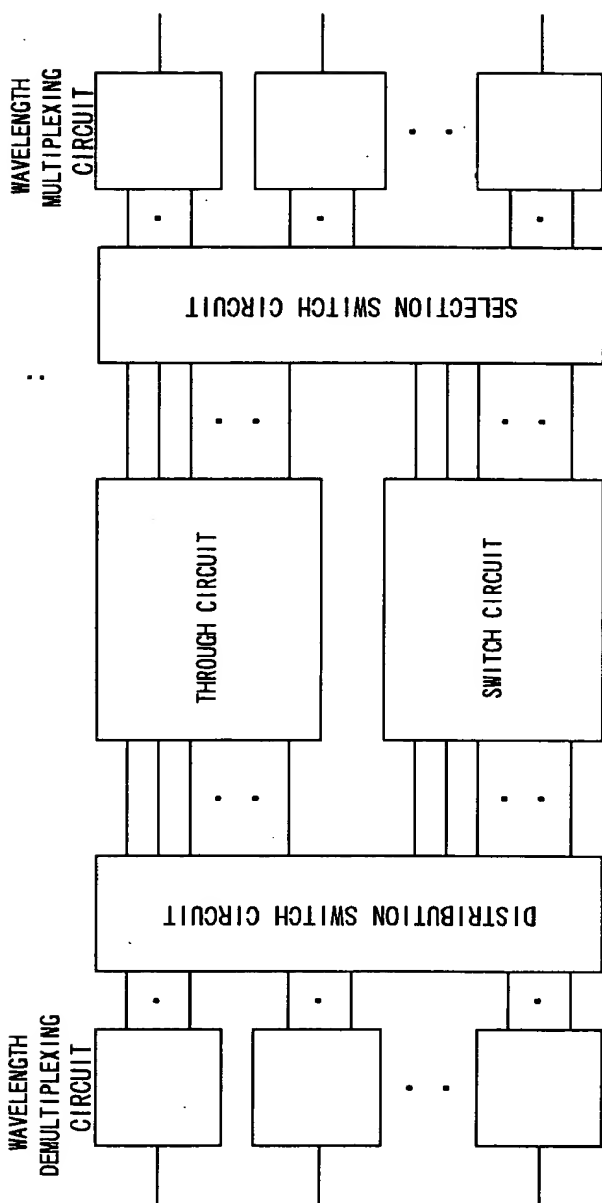


FIG. 51

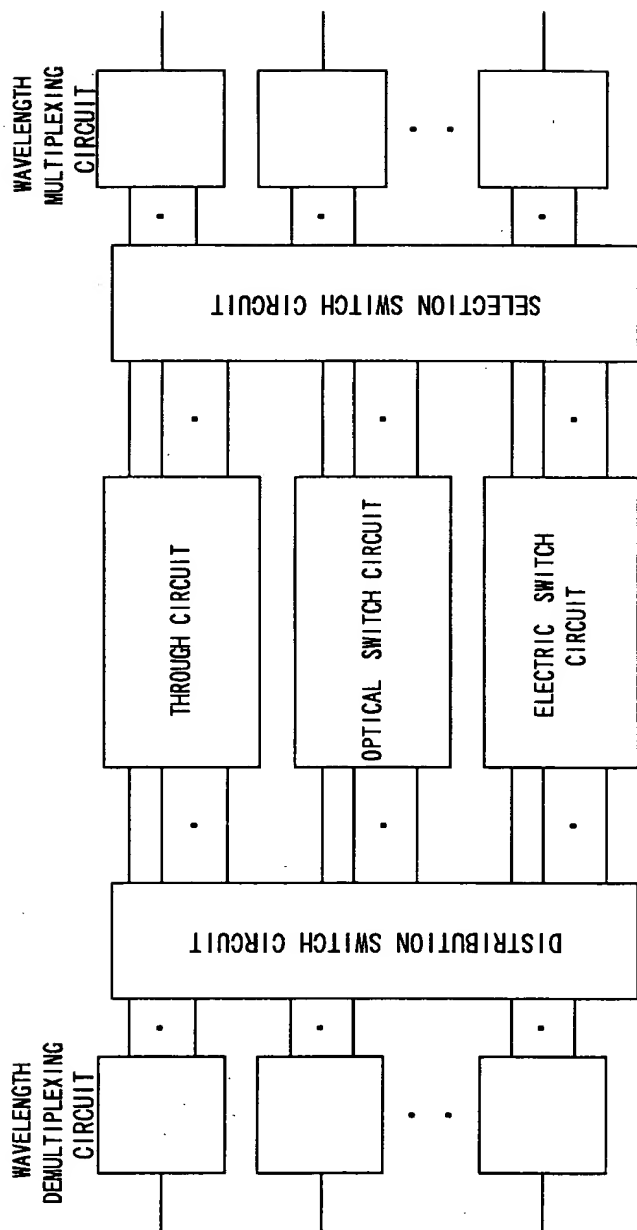
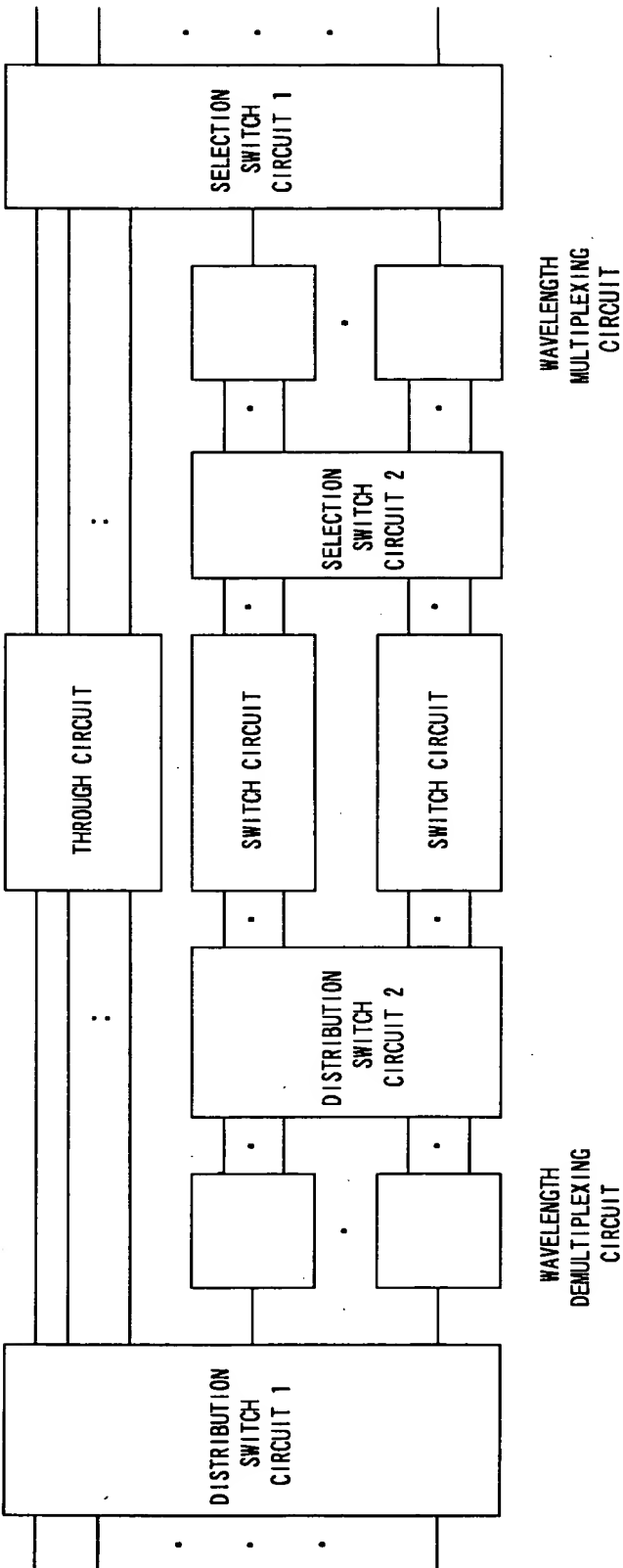


FIG. 52



F1 G. 53

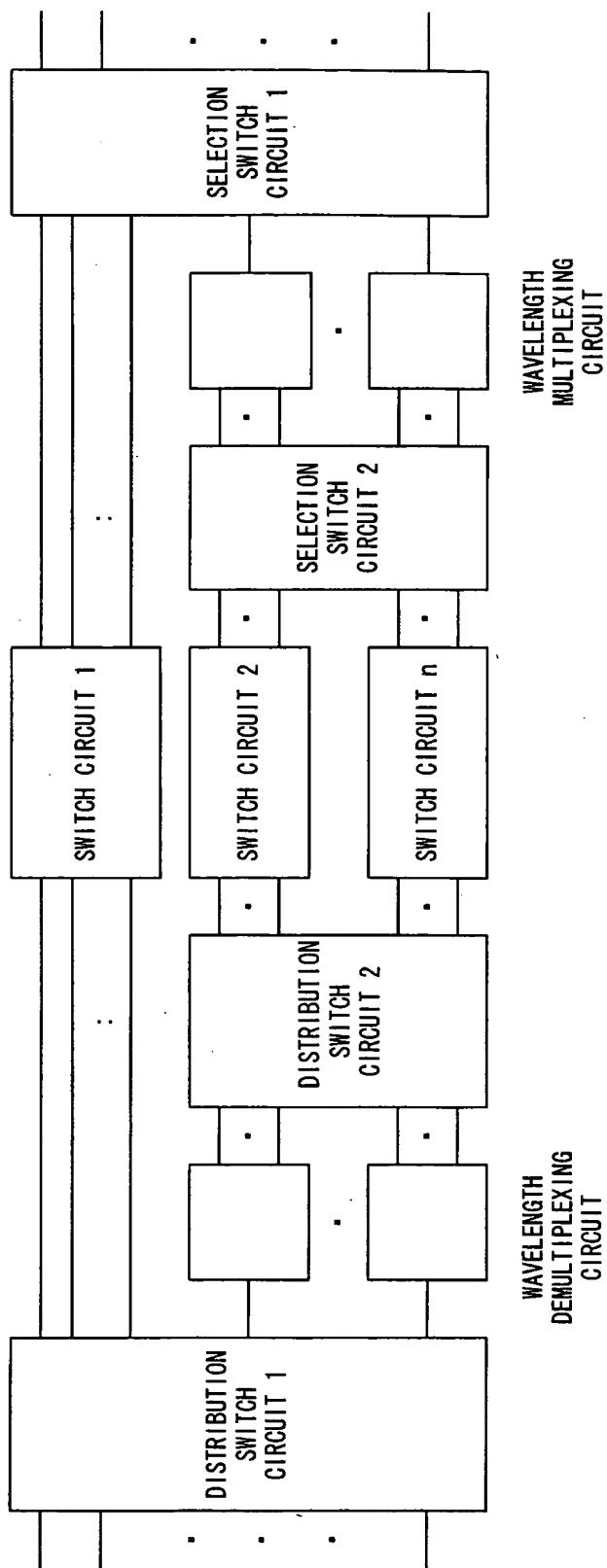


FIG. 54

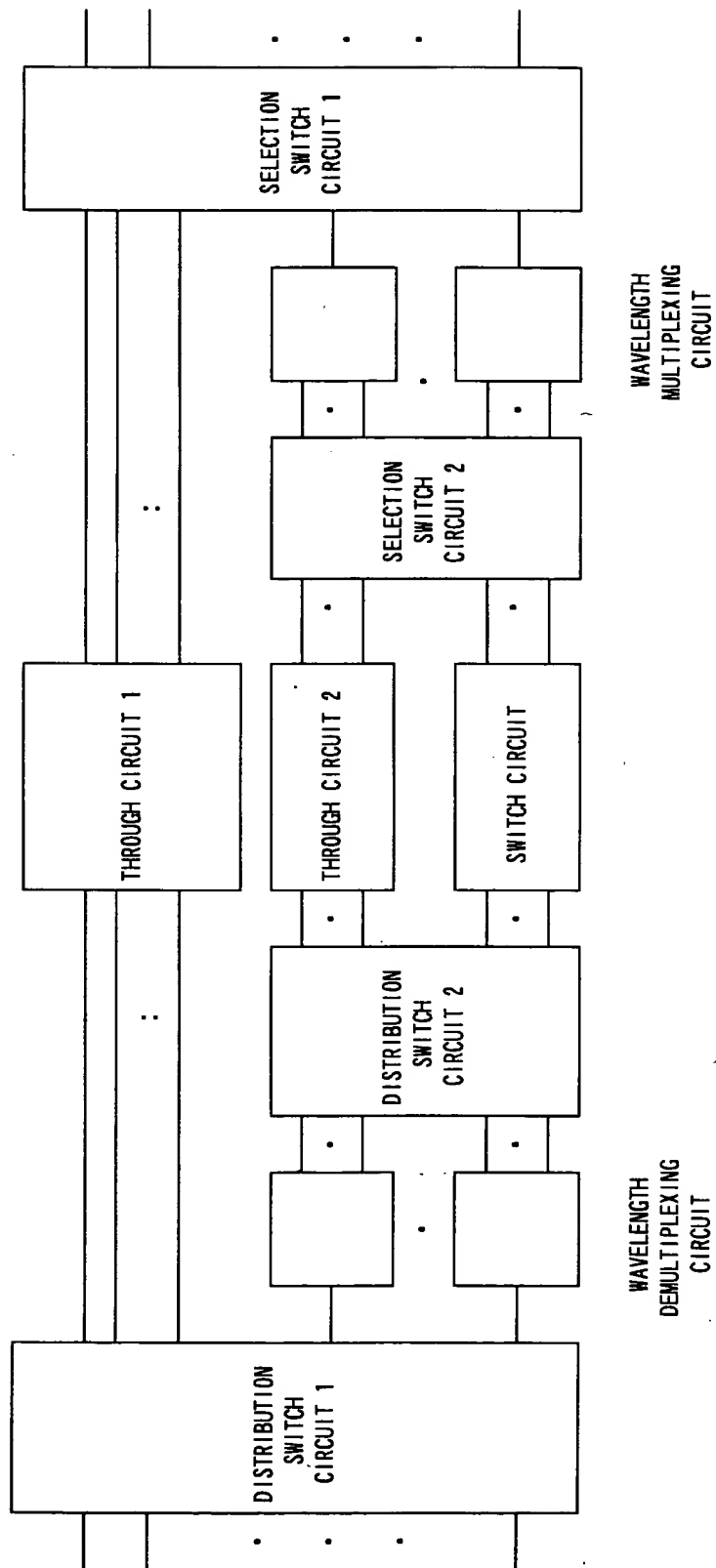


FIG. 55

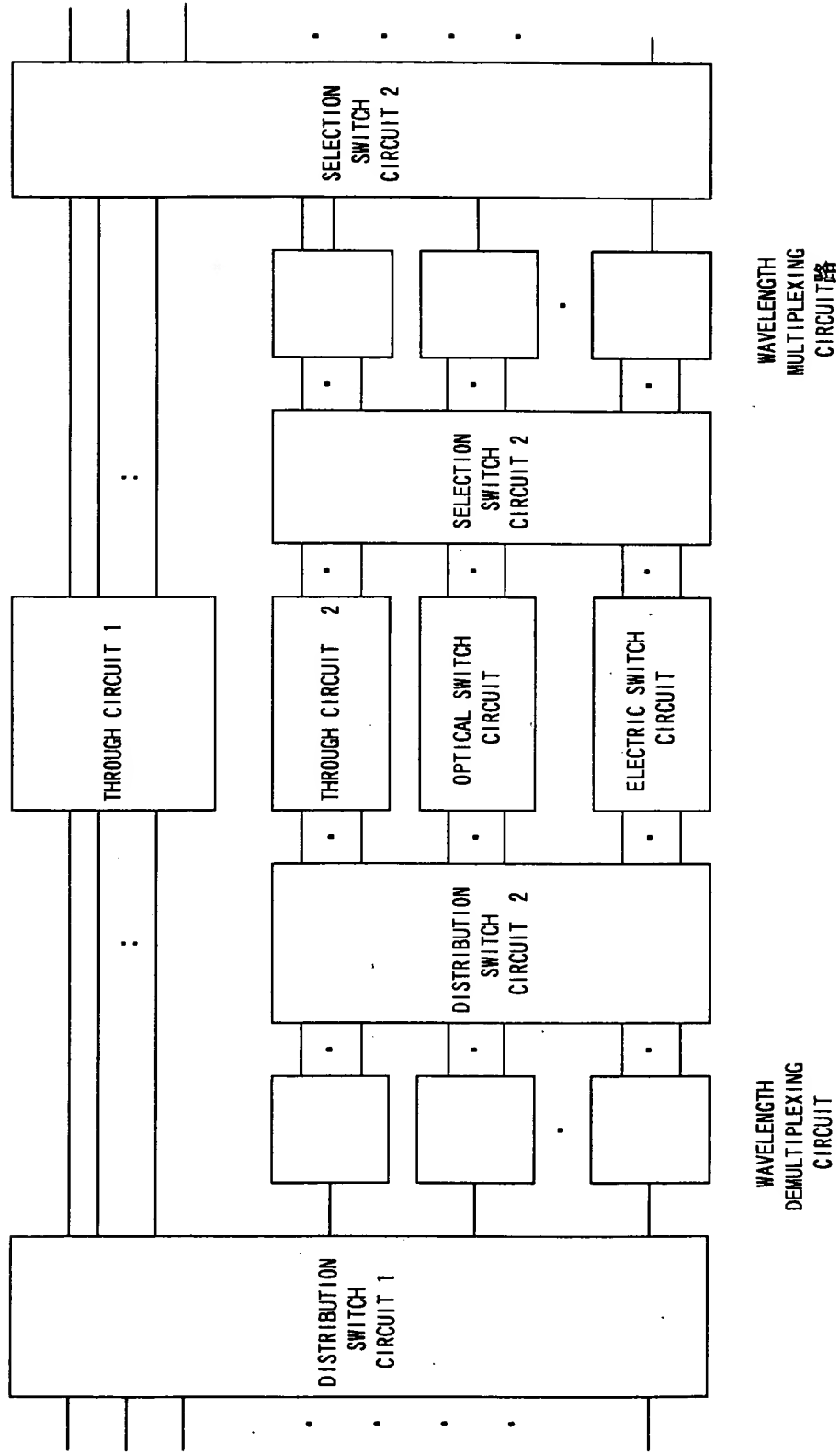
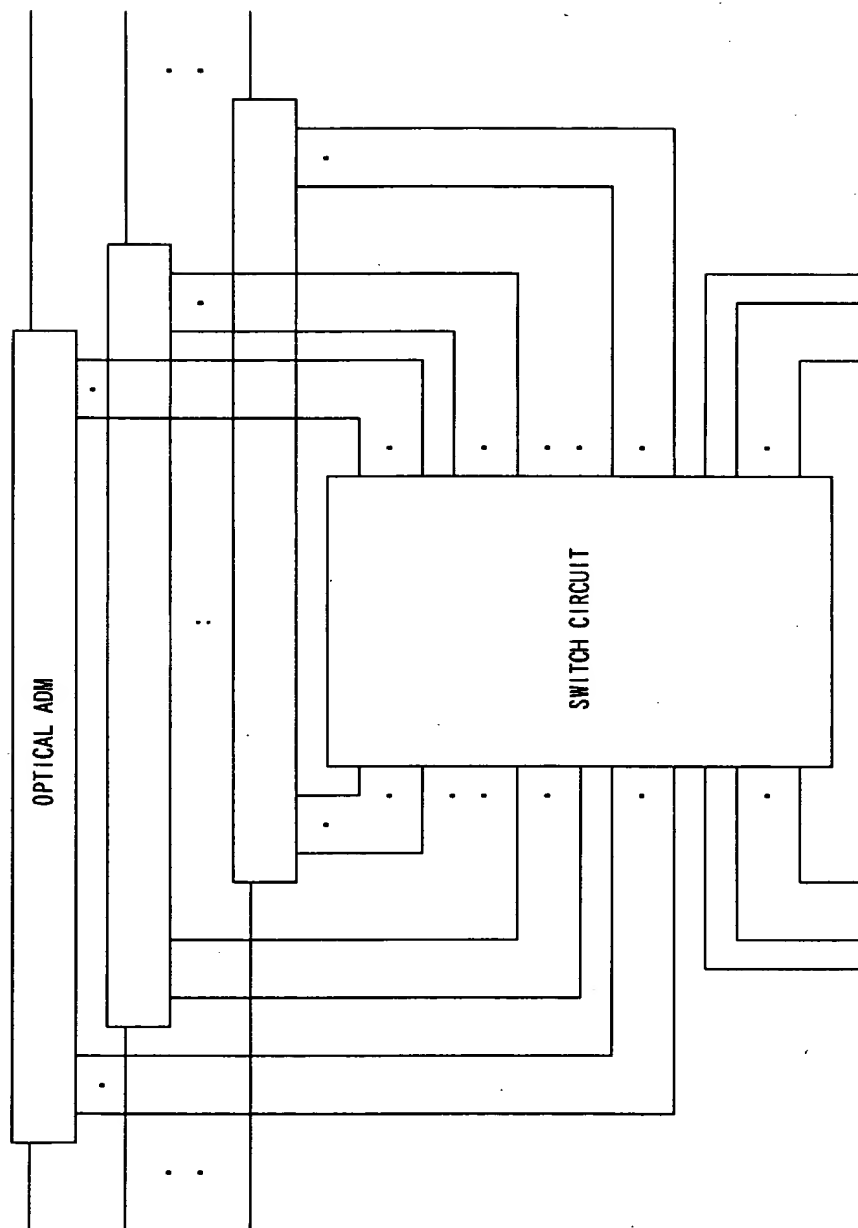


FIG. 56

FIG. 57



F. I. G. 58

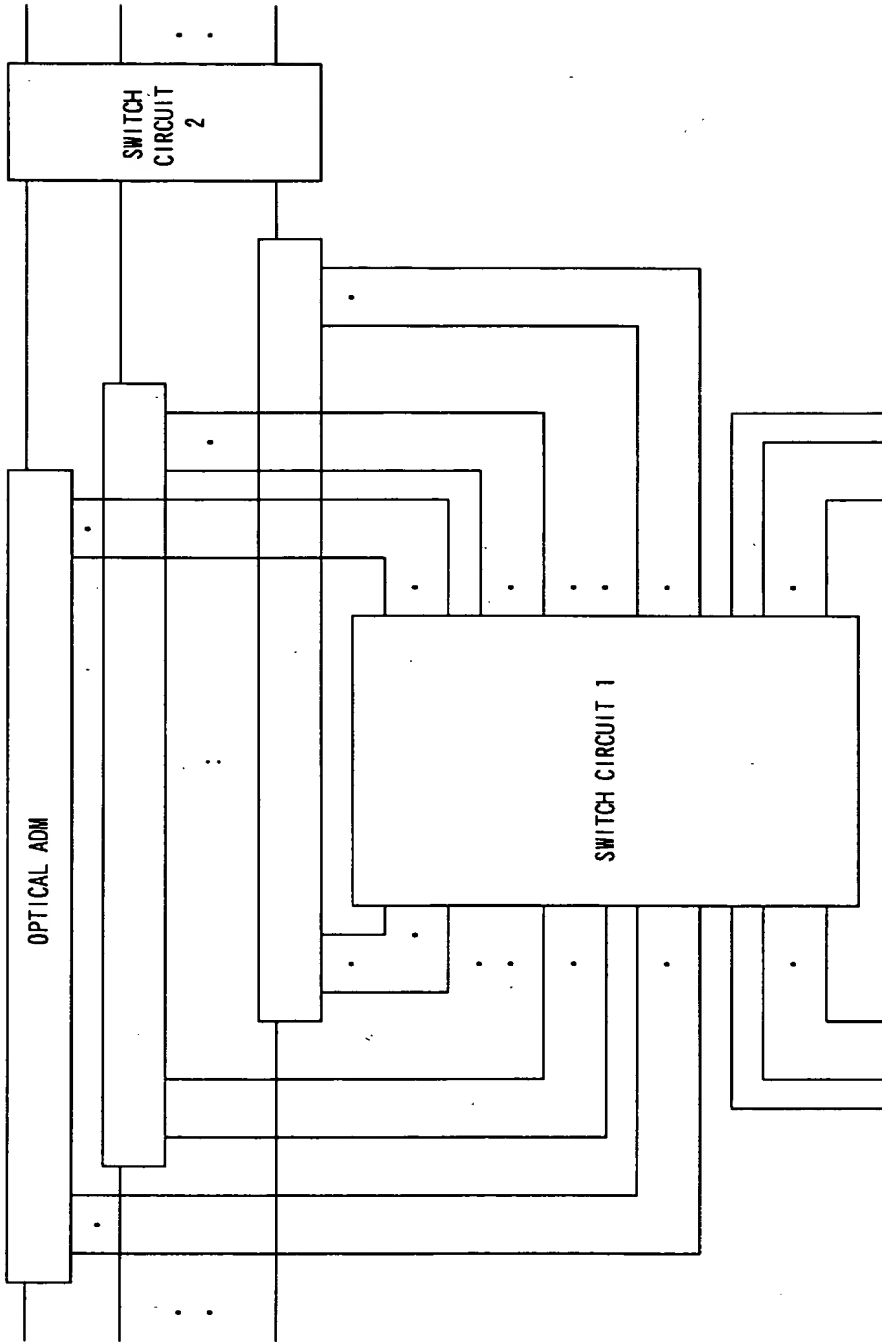


FIG. 59

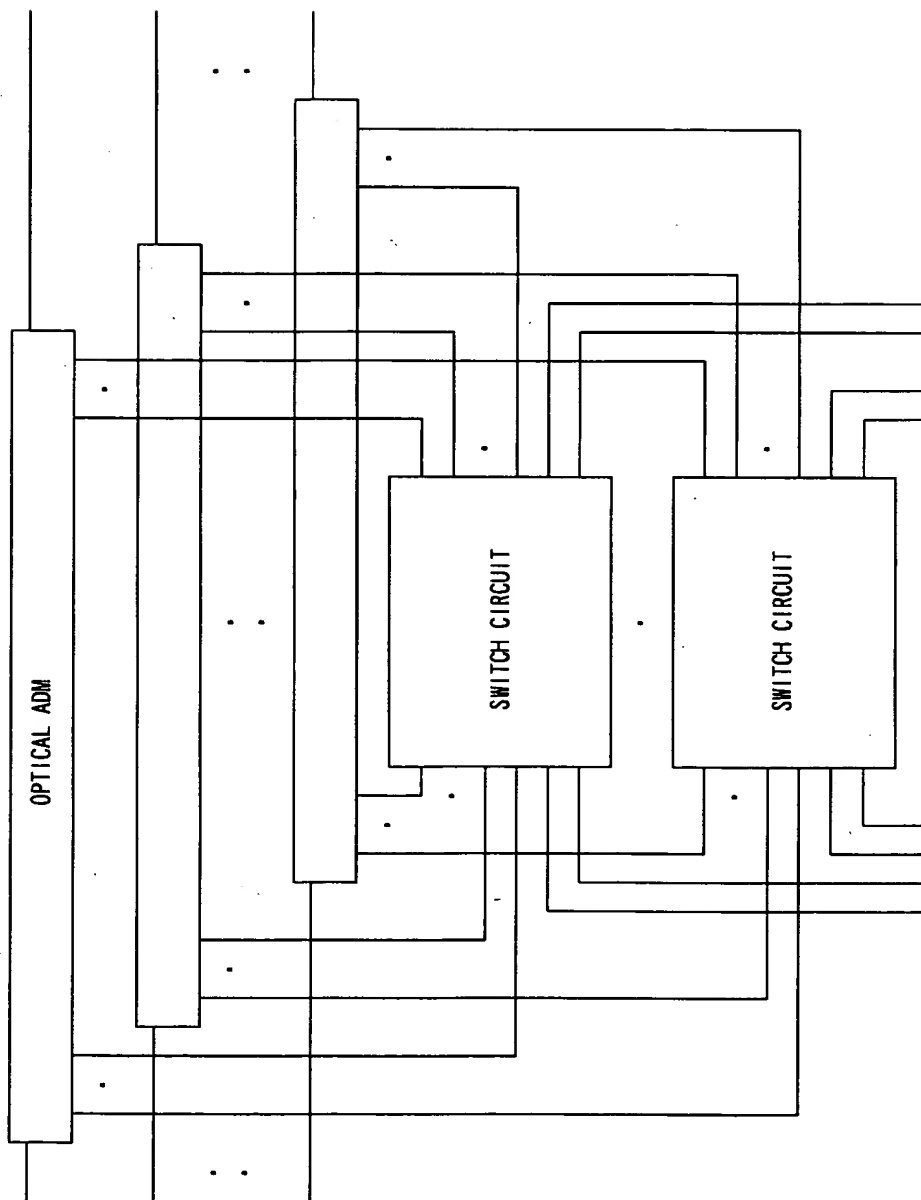


FIG. 60

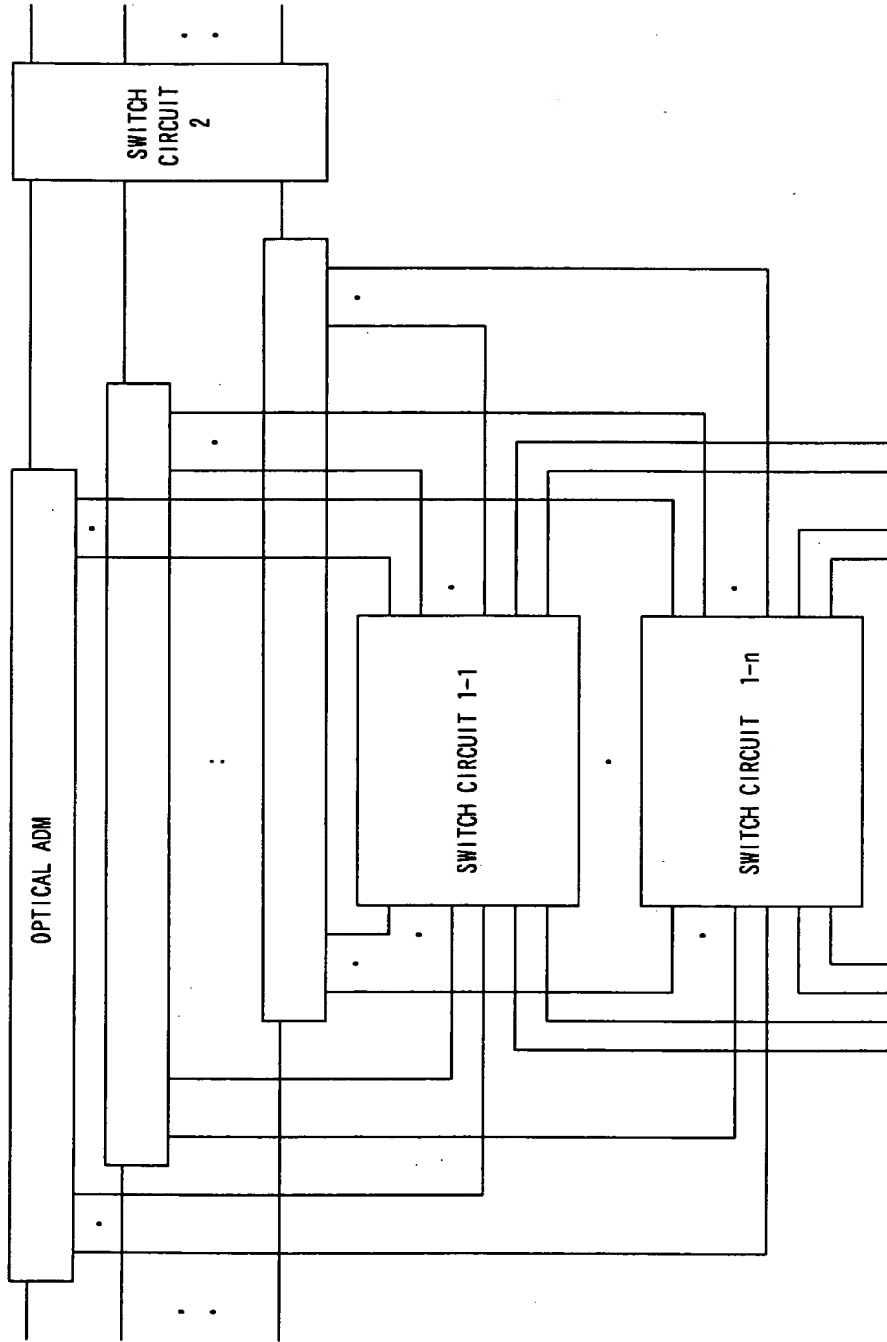


FIG. 61

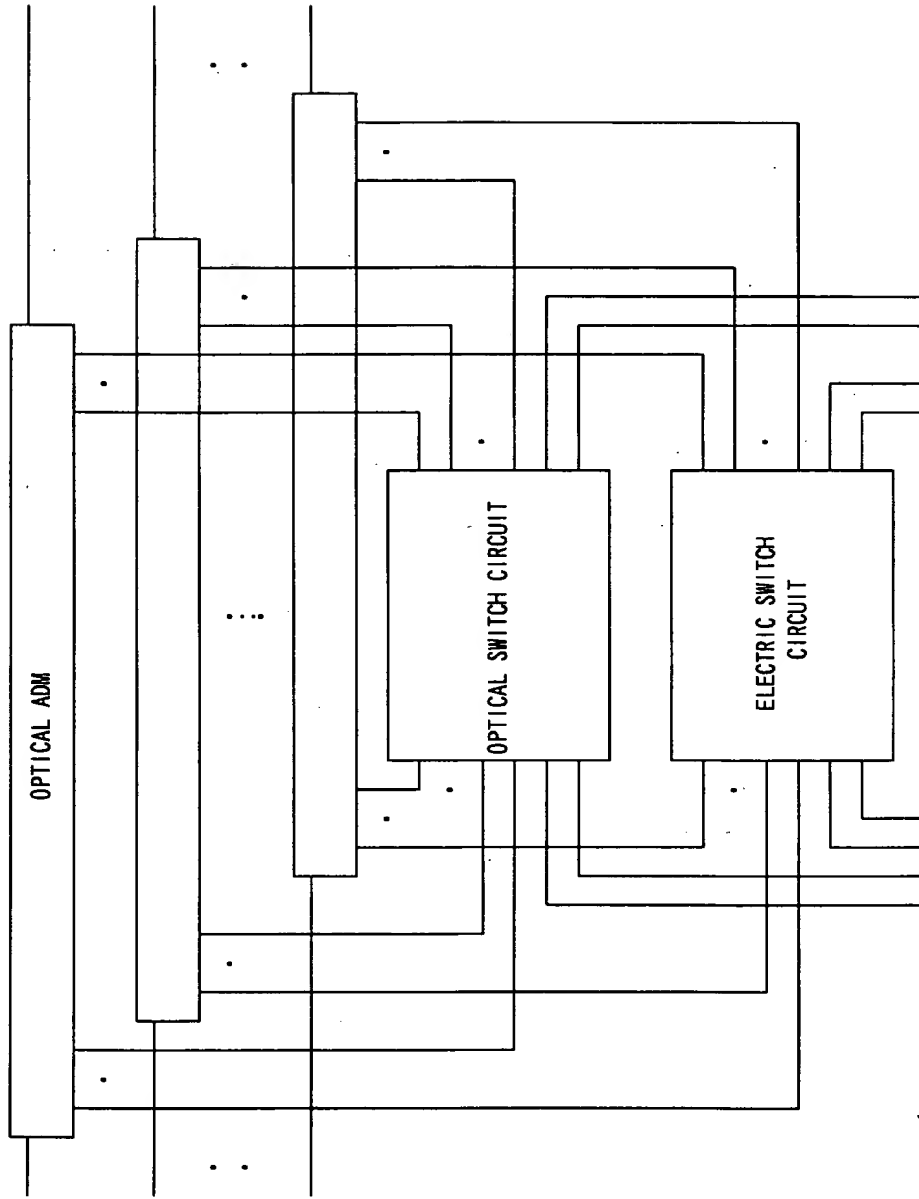


FIG. 62

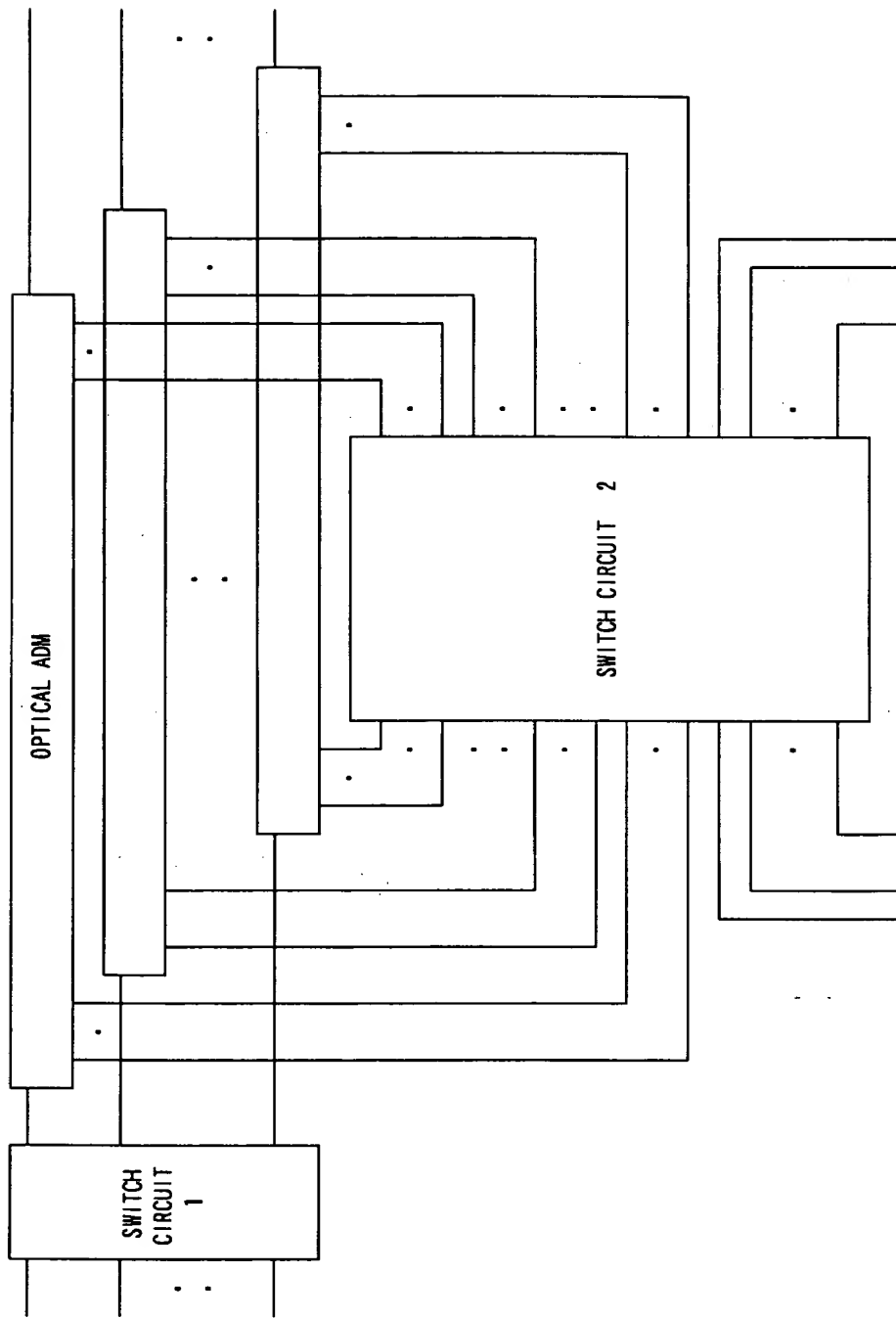


FIG. 64

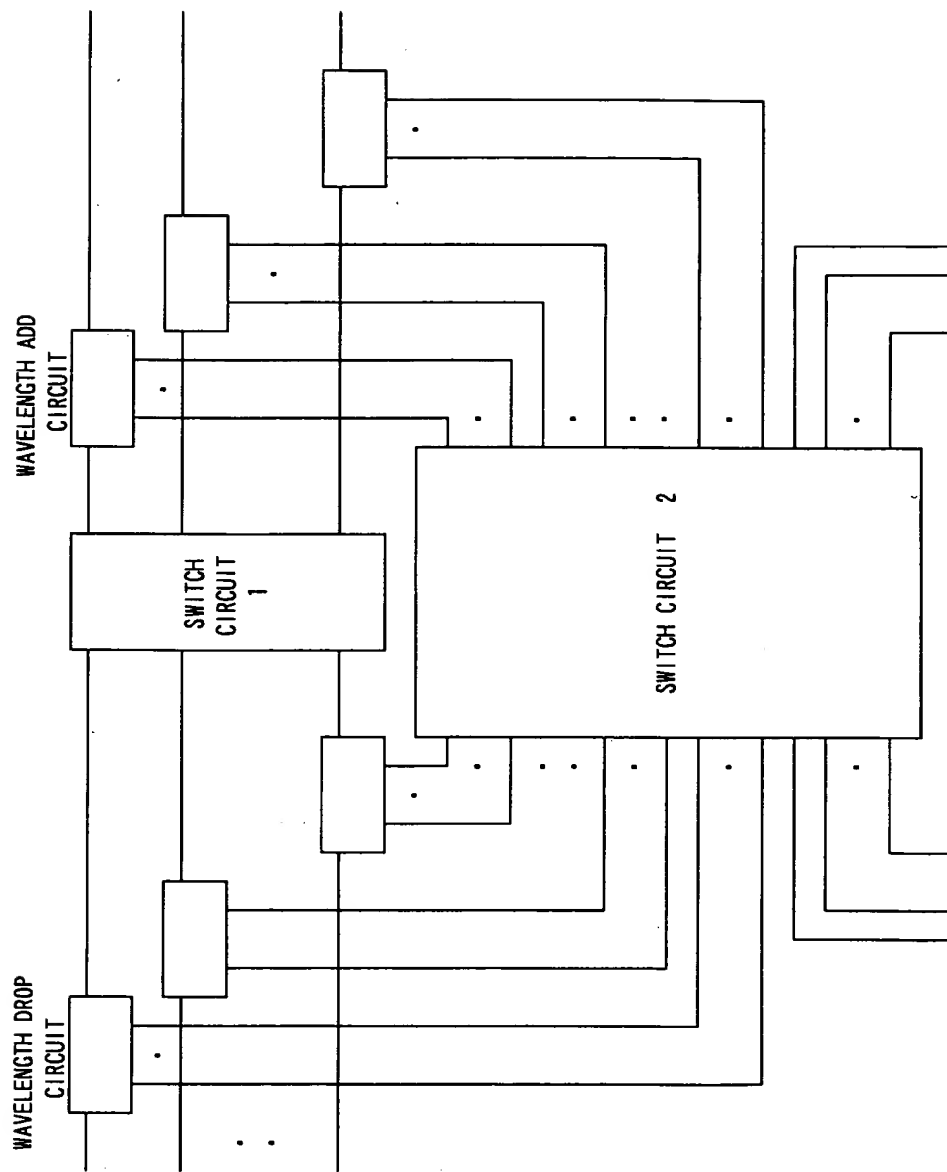


FIG. 65

The diagram illustrates the internal structure of an Optical Add-Drop Multiplexer (ADM). On the left, a vertical bar represents the 'OPTICAL ADM' input/output. Multiple lines enter from the left and are distributed to a series of horizontal bars representing input channels. These channels are connected to a central processing area containing three main blocks: a 'DISTRIBUTION SWITCH CIRCUIT' on the left, a 'SELECTION SWITCH CIRCUIT' on the right, and two 'SWITCH CIRCUIT' blocks in the center. The 'DISTRIBUTION SWITCH CIRCUIT' and 'SELECTION SWITCH CIRCUIT' are connected to the input channels. The 'SWITCH CIRCUIT' blocks are connected to the output channels on the right. The diagram shows a complex interconnection of lines between these components, representing the optical switching and routing process.

FIG. 66

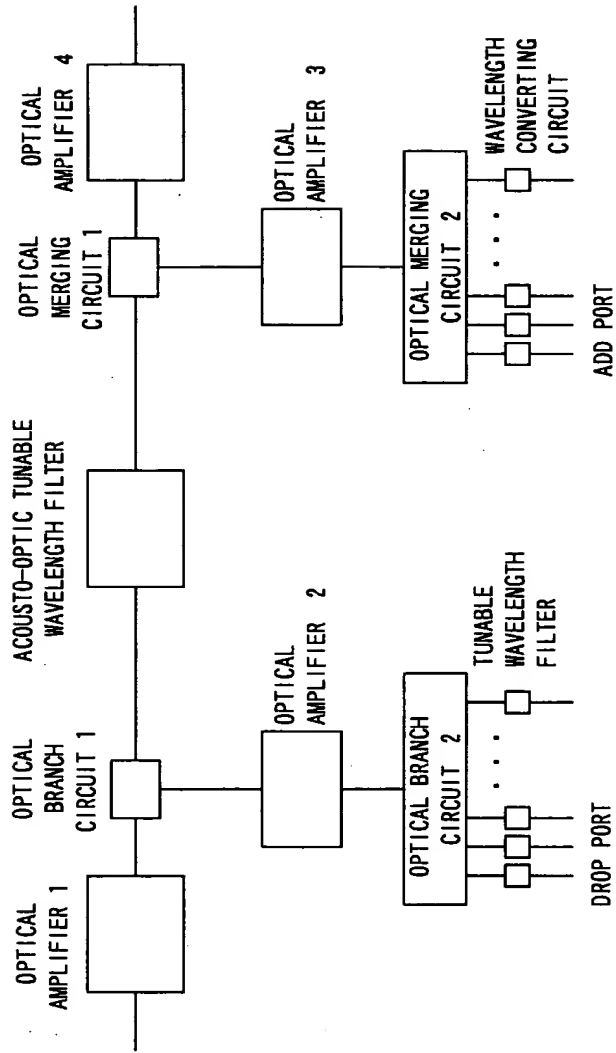


FIG. 67

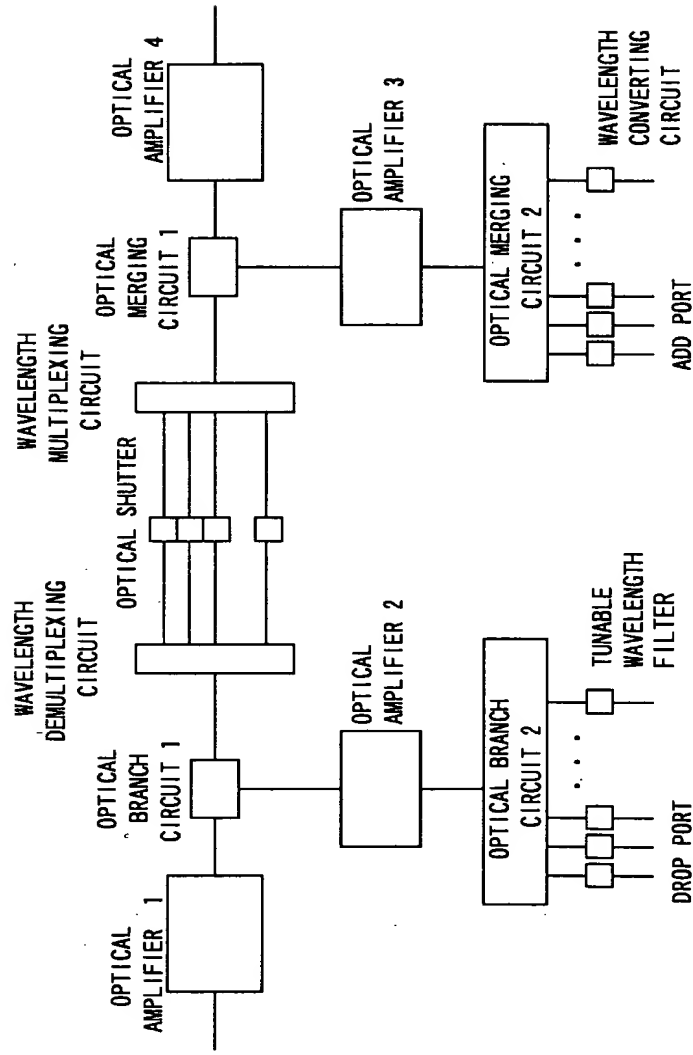


FIG. 68